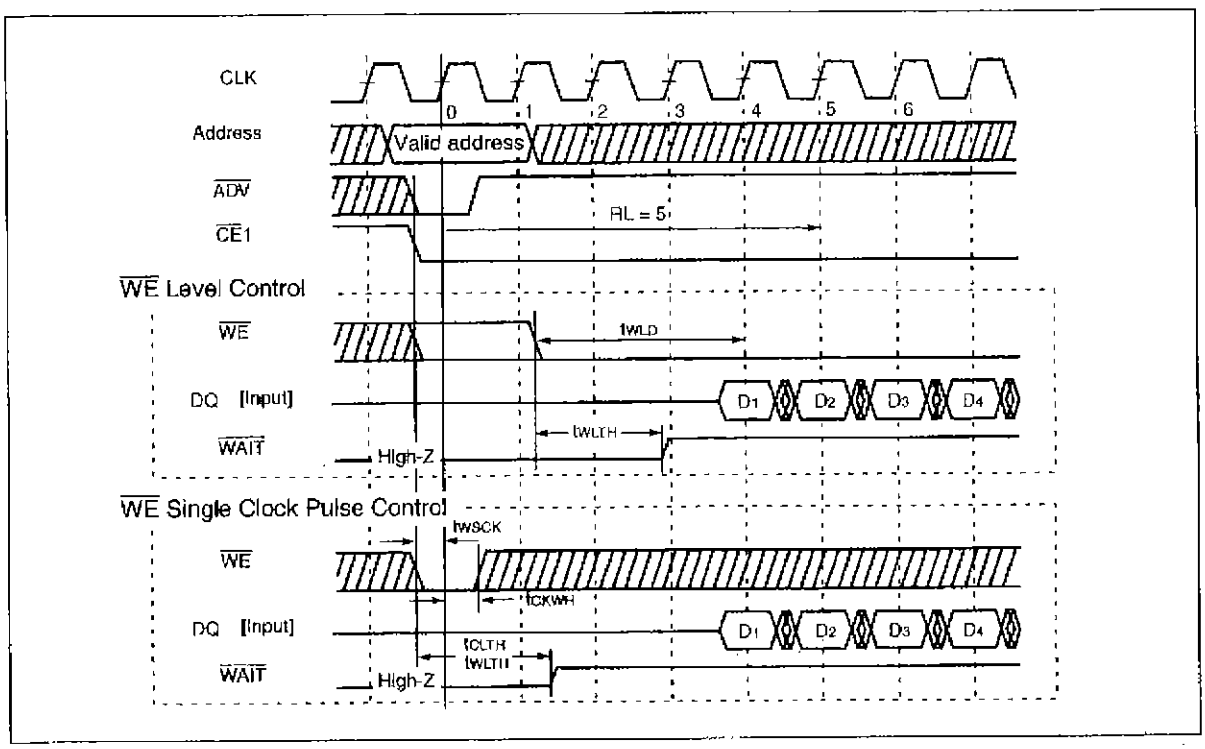
• **Write control**

The device has two types of $\overline{WE}$ signal control method, "$\overline{WE}$ Level Control" and "$\overline{WE}$ Single Clock Pulse Control", for synchronous burst write operation. It is configured through CR set sequence.

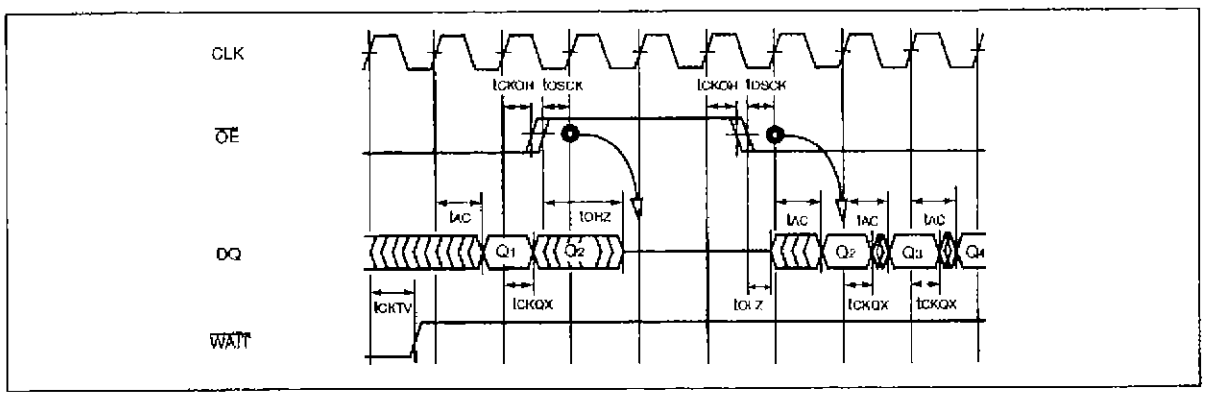


• **Burst Read Suspend**

Burst read operation can be suspended by $\overline{OE}$ High pulse. During burst read operation, $\overline{OE}$ brought to High from Low suspends burst read operation. Once $\overline{OE}$ is brought to High with the specified setup time against clock where the data being suspended, the device internal counter is suspended, and the data output becomes high impedance after specified time duration. It is inhibited to suspend the first data output at the beginning of burst read.

$\overline{OE}$ brought to Low from High resumes burst read operation. Once $\overline{OE}$ is brought to Low, data output becomes valid after specified time duration, and internal address counter is reactivated. The last data output being suspended as the result of $\overline{OE}$ = H and first data output as the result of $\overline{OE}$ = L are from the same address.

In order to guarantee to output last data before suspension and first data after resumption, the specified minimum value of $\overline{OE}$ hold time and setup time against clock edge must be satisfied respectively.



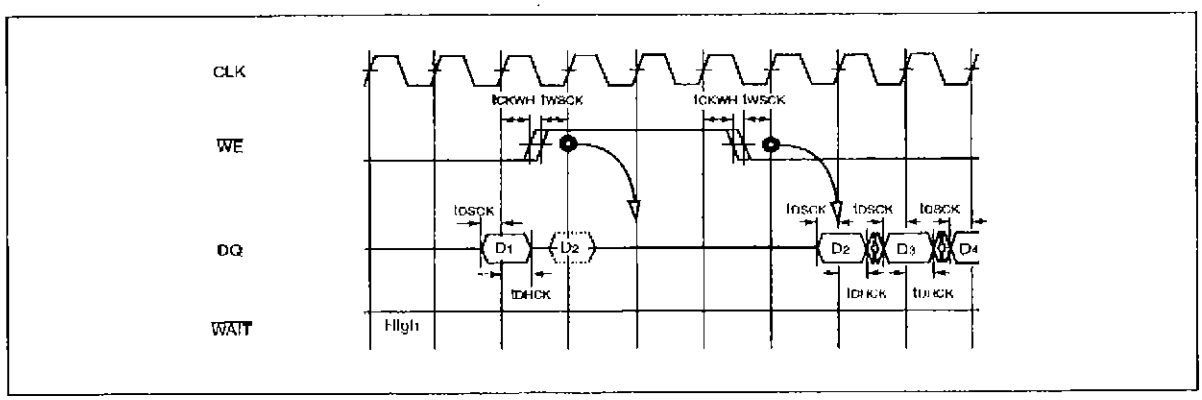
• **Burst Write Suspend**

Burst write operation can be suspended by $\overline{WE}$ High pulse. During burst write operation, $\overline{WE}$ brought to High from Low suspends burst write operation. Once $\overline{WE}$ is brought to High with the specified setup time against clock where the data being suspended, device internal counter is suspended, data input is ignored. It is inhibited to suspend the first data input at the beginning of burst write.

$\overline{WE}$ brought to Low from High resumes burst write operation. Once $\overline{WE}$ is brought to Low, data input becomes valid after specified time duration, and internal address counter is reactivated. The write address of the cycle where data being suspended and the first write address as the result of $\overline{WE}$ = L are the same address.

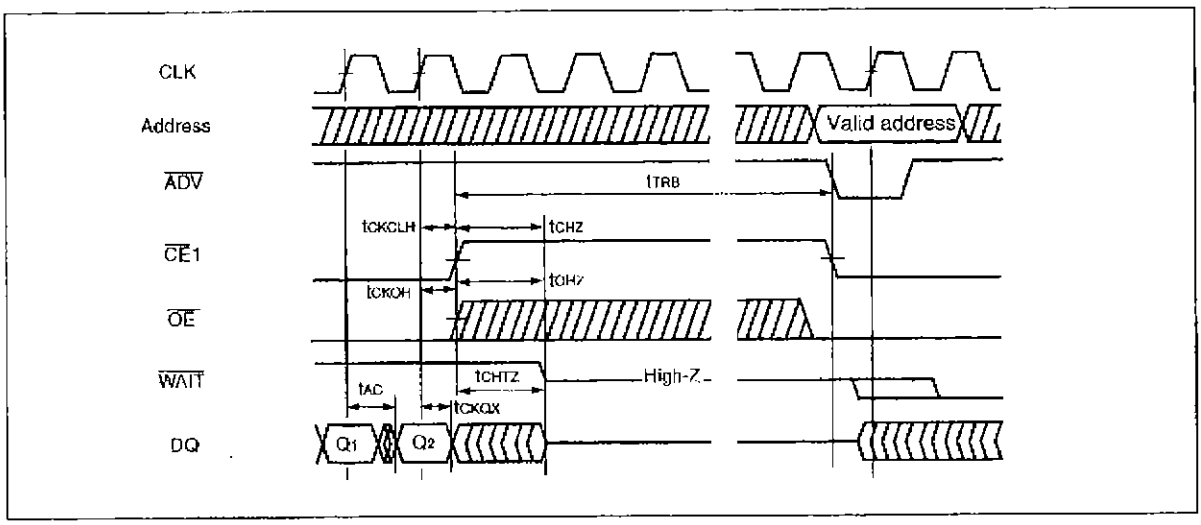
In order to guarantee to latch the last data input before suspension and first data input after resumption, the specified minimum value of $\overline{WE}$ hold time and setup time against clock edge must be satisfied respectively.

Burst write suspend function is available when the device is operating in $\overline{WE}$ level controlled burst write only.



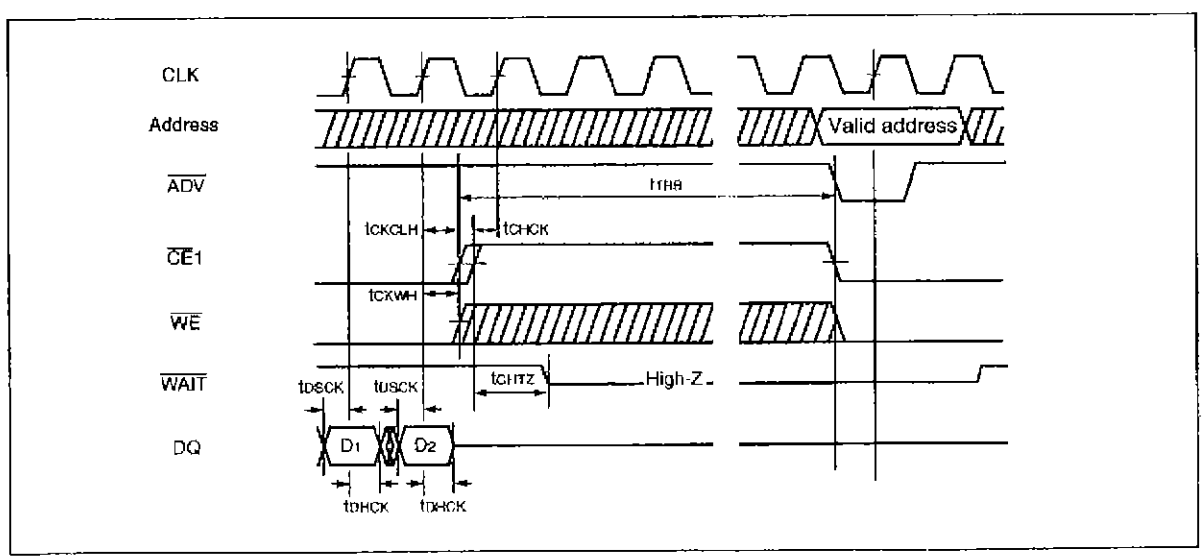
• **Burst Read Termination**

Burst read operation can be terminated by $\overline{CE}1$ brought to High. If BL is set on Continuous, burst read operation is continued endless unless terminated by $\overline{CE}1$ = H. It is inhibited to terminate burst read before first data output is completed. In order to guarantee last data output, the specified minimum value of $\overline{CE}1$ = L hold time from clock edge must be satisfied. After termination, the specified minimum recovery time is required to start new access.



• **Burst Write Termination**

Burst write operation can be terminated by $\overline{CE}1$ brought to High. If BL is set on Continuous, burst write operation is continued endless unless terminated by $\overline{CE}1$ = H. It is inhibited to terminate burst write before first data input is completed. In order to guarantee last data input being latched, the specified minimum values of $\overline{CE}1$ = L hold time from clock edge must be satisfied. After termination, the specified minimum recovery time is required to start new access.



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Voltage of V_{DD} Supply Relative to V_{SS} *	V_{DD}	− 0.5	+ 3.6	V
Voltage at Any Pin Relative to V_{SS} *	V_{IN}, V_{OUT}	− 0.5	+ 3.6	V
Short Circuit Output Current *	I_{OUT}	− 50	+ 50	mA
Storage Temperature	T_{STG}	− 55	+ 125	°C

* : All voltages are referenced to V_{SS} = 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min	Max	
Power Supply Voltage*1	V_{DD}	1.65	1.95	V
	V_{SS}	0	0	V
High Level Input Voltage*1, *2	V_{IH}	V_{DD} × 0.8	V_{DD} + 0.2	V
Low Level Input Voltage*1, *3	V_{IL}	− 0.3	V_{DD} × 0.2	V
Ambient Temperature	T_A	− 30	+ 85	°C

*1 : All voltages are referenced to V_{SS} = 0 V.

*2 : Maximum DC voltage on input and I/O pins is V_{DD} + 0.2 V. During voltage transitions, inputs may overshoot to V_{DD} + 1.0 V for the periods of up to 5 ns.

*3 : Minimum DC voltage on input or I/O pins is -0.3 V. During voltage transitions, inputs may undershoot V_{SS} to -1.0 V for the periods of up to 5 ns.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ PACKAGE CAPACITANCE

(f = 1 MHz, T_A = +25 °C)

Parameter	Symbol	Test conditions	Value			Unit
			Min	Typ	Max	
Address Input Capacitance	C_{IN1}	V_{IN} = 0 V	—	—	5	pF
Control Input Capacitance	C_{IN2}	V_{IN} = 0 V	—	—	5	pF
Data Input/Output Capacitance	$C_{I/O}$	V_{IO} = 0 V	—	—	8	pF

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions		Value Min	Value Max	Unit
Input Leakage Current	I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$		−1.0	+1.0	µA
Output Leakage Current	I_{LO}	0 V ≤ V_{OUT} ≤ V_{DD}, Output Disable		−1.0	+1.0	µA
Output High Voltage Level	V_{OH}	V_{DD} = V_{DD} (Min), I_{OH} = −0.5 mA		1.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL} = 1 mA		—	0.4	V
V_{DD} Power Down Current	I_{DDPS}	V_{DD} = V_{DD} (Max), V_{IN} = V_{IH} or V_{IL}, CE2 ≤ 0.2 V	SLEEP	—	10	µA
	I_{DDP4}		4 M-bit Partial	—	40	µA
	I_{DDP8}		8 M-bit Partial	—	50	µA
V_{DD} Standby Current	I_{DDS}	V_{DD} = V_{DD} (Max), V_{IN} (including CLK) = V_{IH} or V_{IL}, $\overline{CE}1$ = CE2 = V_{IH}		—	1.5	mA
	I_{DDS1}	V_{DD} = V_{DD} (Max), V_{IN} (including CLK) ≤ 0.2 V or V_{IN} (including CLK) ≥ V_{DD} − 0.2 V, $\overline{CE}1$ = CE2 ≥ V_{DD} − 0.2 V		—	80	µA
	I_{DDS2}	V_{DD} = V_{DD} (Max), t_{CK} = Min V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{DD} − 0.2 V, $\overline{CE}1$ = CE2 ≥ V_{DD} − 0.2 V		—	200	µA
V_{DD} Active Current	I_{DDA1}	V_{DD} = V_{DD} (Max), V_{IN} = V_{IH} or V_{IL}, $\overline{CE}1$ = V_{IL} and CE2 = V_{IH}, I_{OUT} = 0 mA	t_{RC}/t_{WC} = Min	—	30	mA
	I_{DDA2}		t_{RC}/t_{WC} = 1 µs	—	3	mA
V_{DD} Page Read Current	I_{DDA3}	V_{DD} = V_{DD} (Max), V_{IN} = V_{IH} or V_{IL}, $\overline{CE}1$ = V_{IL} and CE2 = V_{IH}, I_{OUT} = 0 mA, t_{PRC} = Min		—	10	mA
V_{DD} Burst Access Current	I_{DDA4}	V_{DD} = V_{DD} (Max), V_{IN} = V_{IH} or V_{IL}, $\overline{CE}1$ = V_{IL} and CE2 = V_{IH}, t_{CK} = t_{CK} (Min), BL = Continuous, I_{OUT} = 0 mA		—	15	mA

Notes :
- All voltages are referenced to V_{SS} = 0 V.
- I_{DD} depends on the output termination, load conditions, and AC characteristics.
- After power on, initialization following POWER-UP timing is required. DC characteristics are guaranteed after the initialization.

2. AC Characteristics

(1) Asynchronous Read Operation (Page mode)

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Read Cycle Time	t_{RC}	70	1000	ns	*1, *2
$\overline{CE1}$ Access Time	t_{CE}	—	70	ns	*3
$\overline{OE}$ Access Time	t_{OE}	—	40	ns	*3
Address Access Time	t_{AA}	—	70	ns	*3, *5
$\overline{ADV}$ Access Time	t_{AV}	—	70	ns	*3
$\overline{LB}$, $\overline{UB}$ Access Time	t_{BA}	—	30	ns	*3
Page Address Access Time	t_{PAA}	—	20	ns	*3, *6
Page Read Cycle Time	t_{PRC}	20	1000	ns	*1, *6, *7
Output Data Hold Time	t_{OH}	5	—	ns	*3
$\overline{CE1}$ Low to Output Low-Z	t_{CLZ}	5	—	ns	*4
$\overline{OE}$ Low to Output Low-Z	t_{OLZ}	10	—	ns	*4
$\overline{LB}$, $\overline{UB}$ Low to Output Low-Z	t_{BLZ}	0	—	ns	*4
$\overline{CE1}$ High to Output High-Z	t_{CHZ}	—	14	ns	*3
$\overline{OE}$ High to Output High-Z	t_{OHZ}	—	14	ns	*3
$\overline{LB}$, $\overline{UB}$ High to Output High-Z	t_{BHZ}	—	14	ns	*3
Address Setup Time to $\overline{CE1}$ Low	t_{ASC}	−5	—	ns	
Address Setup Time to $\overline{OE}$ Low	t_{ASO}	10	—	ns	
$\overline{ADV}$ Low Pulse Width	t_{VPL}	10	—	ns	*8
$\overline{ADV}$ High Pulse Width	t_{VPH}	15	—	ns	*8
Address Setup Time to $\overline{ADV}$ High	t_{ASV}	5	—	ns	
Address Hold Time from $\overline{ADV}$ High	t_{AHV}	10	—	ns	
Address Invalid Time	t_{AX}	—	10	ns	*5, *9
Address Hold Time from $\overline{CE1}$ High	t_{CHAH}	−5	—	ns	*10
Address Hold Time from $\overline{OE}$ High	t_{OHAH}	−5	—	ns	
$\overline{WE}$ High to $\overline{OE}$ Low Time for Read	t_{WHOL}	15	1000	ns	*11
$\overline{CE1}$ High Pulse Width	t_{CP}	15	—	ns	

*1 : Maximum value is applicable if $\overline{CE1}$ is kept at Low without change of address input of A_{20} to A_3.

*2 : Address should not be changed within minimum t_{RC}.

*3 : The output load 50 pF with 50 Ω termination to $V_{DD} \times 0.5$ V.

*4 : The output load 5 pF without any other load.

*5 : Applicable to A_{20} to A_3 when $\overline{CE1}$ is kept at Low.

*6 : Applicable only to A_2, A_1 and A_0 when $\overline{CE1}$ is kept at Low for the page address access.

(Continued)

(Continued)

*7 : In case Page Read Cycle is continued with keeping $\overline{CE}1$ stays Low, $\overline{CE}1$ must be brought to High within 4 µs. In other words, Page Read Cycle must be closed within 4 µs.

*8 : t_{VPL} is specified from the falling edge of either $\overline{CE}1$ or $\overline{ADV}$ whichever comes late. The sum of t_{VPL} and t_{VPH} must be equal or greater than t_{RC} for each access.

*9 : Applicable to address access when at least two of address inputs are switched from previous state.

*10 : t_{RC} (Min) and t_{PRC} (Min) must be satisfied.

*11 : If actual value of t_{WHOL} is shorter than specified minimum values, the actual t_{AA} of following Read may become longer by the amount of subtracting actual value from specified minimum value.

(2) Asynchronous Write Operation

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Write Cycle Time	t_{WC}	70	1000	ns	*1, *2
Address Setup Time	t_{AS}	0	—	ns	*3
$\overline{ADV}$ Low Pulse Width	t_{VPL}	10	—	ns	*4
$\overline{ADV}$ High Pulse Width	t_{VPH}	15	—	ns	*4
Address Setup Time to $\overline{ADV}$ High	t_{ASV}	5	—	ns	
Address Hold Time from $\overline{ADV}$ High	t_{AHV}	10	—	ns	
$\overline{CE}1$ Write Pulse Width	t_{CW}	45	—	ns	*3
$\overline{WE}$ Write Pulse Width	t_{WP}	45	—	ns	*3
$\overline{LB}$, $\overline{UB}$ Write Pulse Width	t_{BW}	45	—	ns	*3
$\overline{LB}$, $\overline{UB}$ Byte Mask Setup Time	t_{BS}	–5	—	ns	*5
$\overline{LB}$, $\overline{UB}$ Byte Mask Hold Time	t_{BH}	–5	—	ns	*6
Write Recovery Time	t_{WR}	0	—	ns	*7
$\overline{CE}1$ High Pulse Width	t_{CP}	15	—	ns	
$\overline{WE}$ High Pulse Width	t_{WHP}	15	1000	ns	
$\overline{LB}$, $\overline{UB}$ High Pulse Width	t_{BHP}	15	1000	ns	
Data Setup Time	t_{DS}	15	—	ns	
Data Hold Time	t_{DH}	0	—	ns	
$\overline{OE}$ High to $\overline{CE}1$ Low Setup Time for Write	t_{OHCL}	–5	—	ns	*8
$\overline{OE}$ High to Address Setup Time for Write	t_{OES}	0	—	ns	*9
$\overline{LB}$ and $\overline{UB}$ Write Pulse Overlap	t_{BWO}	30	—	ns	

*1 : Maximum value is applicable if $\overline{CE}1$ is kept at Low without any address change.

*2 : Minimum value must be equal or greater than the sum of write pulse width (t_{CW}, t_{WP} or t_{BW}) and write recovery time (t_{WR}).

*3 : Write pulse width is defined from High to Low transition of $\overline{CE}1$, $\overline{WE}$, $\overline{LB}$, or $\overline{UB}$, whichever occurs last.

*4: t_{VPL} is specified from the falling edge of either $\overline{CE}1$ or $\overline{ADV}$ whichever comes late. The sum of t_{VPL} and t_{VPH} must be equal or greater than t_{WC} for each access.

*5: Applicable for byte mask only. Byte mask setup time is defined from the High to Low transition of $\overline{CE}1$ or $\overline{WE}$ whichever occurs last.

*6: Applicable for byte mask only. Byte mask hold time is defined from the Low to High transition of $\overline{CE}1$ or $\overline{WE}$ whichever occurs first.

*7: Write recovery time is defined from Low to High transition of $\overline{CE}1$, $\overline{WE}$, $\overline{LB}$, or $\overline{UB}$, whichever occurs first.

*8: If $\overline{OE}$ is Low after minimum t_{OHCL}, read cycle is initiated. In other word, $\overline{OE}$ must be brought to High within 5 ns after $\overline{CE}1$ is brought to Low.

*9: If $\overline{OE}$ is Low after new address input, read cycle is initiated. In other word, $\overline{OE}$ must be brought to High at the same time or before new address is valid.

(3) Synchronous Operation - Clock Input (Burst mode)

(At recommended operating conditions unless otherwise noted)

Parameter		Symbol	Value		Unit	Notes
			Min	Max		
Clock Period	RL = 5	t_{CK}	15	—	ns	*1
	RL = 4		20	—	ns	*1
	RL = 3		30	—	ns	*1
Clock High Pulse Width		t_{CKH}	5	—	ns	
Clock Low Pulse Width		t_{CKL}	5	—	ns	
Clock Transition Time		t_{CKT}	—	3	ns	*2

*1: Clock period is defined between valid clock edges.

*2: Clock transition time is defined between V_{IH} (Min) and V_{IL} (Max)

(4) Synchronous Operation - Address Latch (Burst mode)

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Address Setup Time to $\overline{CE}1$ Low	t_{ASCL}	−5	—	ns	*1
Address Setup Time to $\overline{ADV}$ Low	t_{ASVL}	−5	—	ns	*2
Address Hold Time from $\overline{ADV}$ High	t_{AHV}	10	—	ns	
$\overline{ADV}$ Low Pulse Width	t_{VPL}	10	—	ns	*3
$\overline{ADV}$ Low Setup Time to CLK	t_{VSCK}	7	—	ns	*4
$\overline{CE}1$ Low Setup Time to CLK	t_{CLCK}	7	—	ns	*4
$\overline{ADV}$ Low Hold Time from CLK	t_{CKVH}	1	—	ns	*4
Burst End $\overline{ADV}$ High Hold Time from CLK	t_{VHVL}	15	—	ns	

*1: t_{ASCL} is applicable if $\overline{CE}1$ is brought to Low after $\overline{ADV}$ is brought to Low.

*2: t_{ASVL} is applicable if $\overline{ADV}$ is brought to Low after $\overline{CE}1$ is brought to Low.

*3: t_{VPL} is specified from the falling edge of either $\overline{CE}1$ or $\overline{ADV}$ whichever comes late.

*4: Applicable to the 1st valid clock edge.

(5) Synchronous Read Operation (Burst mode)

(At recommended operating conditions unless otherwise noted)

Parameter		Symbol	Value		Unit	Notes
			Min	Max		
Burst Read Cycle Time		t_{RCB}	—	8000	ns	
CLK Access Time		t_{AC}	—	12	ns	*1
Output Hold Time from CLK		t_{CKQX}	3	—	ns	*1
$\overline{CE}1$ Low to $\overline{WAIT}$ Low		t_{CLTL}	5	20	ns	*1
$\overline{OE}$ Low to $\overline{WAIT}$ Low		t_{OLTL}	0	20	ns	*1, *2
CLK to $\overline{WAIT}$ Valid Time		t_{CKTV}	—	12	ns	*1, *3
$\overline{WAIT}$ Valid Hold Time from CLK		t_{CKTX}	3	—	ns	*1
$\overline{CE}1$ Low to Output Low-Z		t_{CLZ}	5	—	ns	*4
$\overline{OE}$ Low to Output Low-Z		t_{OLZ}	10	—	ns	*4
$\overline{LB}$, $\overline{UB}$ Low to Output Low-Z		t_{BLZ}	0	—	ns	*4
$\overline{CE}1$ High to Output High-Z		t_{CHZ}	—	14	ns	*1
$\overline{OE}$ High to Output High-Z		t_{OHZ}	—	14	ns	*1
$\overline{LB}$, $\overline{UB}$ High to Output High-Z		t_{BHZ}	—	14	ns	*1
$\overline{CE}1$ High to $\overline{WAIT}$ High-Z		t_{CHTZ}	—	20	ns	*1
$\overline{OE}$ High to $\overline{WAIT}$ High-Z		t_{OHTZ}	—	20	ns	*1
$\overline{OE}$ Low Setup Time to 1st Data-output		t_{OLQ}	30	—	ns	
$\overline{LB}$, $\overline{UB}$ Setup Time to 1st Data-output		t_{BLQ}	30	—	ns	*5
$\overline{OE}$ Setup Time to CLK		t_{OSCK}	5	—	ns	
$\overline{OE}$ Hold Time from CLK		t_{CKOH}	5	—	ns	
Burst End $\overline{CE}1$ Low Hold Time from CLK		t_{CKCLH}	5	—	ns	
Burst End $\overline{LB}$, $\overline{UB}$ Hold Time from CLK		t_{CKBH}	5	—	ns	
Burst Terminate Recovery Time	BL = 8, 16	t_{TRB}	30	—	ns	*6
	BL = Continuous		70	—	ns	*6

*1: The output load 50 pF with 50 Ω termination to $V_{DD} \times 0.5$ V.

*2: $\overline{WAIT}$ drives High at the beginning depending on $\overline{OE}$ falling edge timing.

*3: t_{CKTV} is guaranteed after t_{OLTL} (Max) from $\overline{OE}$ falling edge and t_{OSCK} must be satisfied.

*4: The output load 5 pF without any other load.

*5: Once $\overline{LB}$ and $\overline{UB}$ are determined, they must not be changed until the end of burst read.

*6: Defined from the Low to High transition of $\overline{CE}1$ to the High to Low transition of either $\overline{ADV}$ or $\overline{CE}1$ whichever occurs late.

(6) Synchronous Write Operation (Burst mode)

(At recommended operating conditions unless otherwise noted)

Parameter		Symbol	Value		Unit	Notes
			Min	Max		
Burst Write Cycle Time		t_{WCB}	—	8000	ns	
Data Setup Time to CLK		t_{DSCK}	7	—	ns	
Data Hold Time from CLK		t_{DHCK}	3	—	ns	
$\overline{WE}$ Low Setup Time to 1st Data Input		t_{WLD}	30	—	ns	
$\overline{LB}$, $\overline{UB}$ Setup Time for Write		t_{BS}	-5	—	ns	*1
$\overline{WE}$ Setup Time to CLK		t_{WSCK}	5	—	ns	
$\overline{WE}$ Hold Time from CLK		t_{CKWH}	5	—	ns	
$\overline{CE1}$ Low to $\overline{WAIT}$ High		t_{CLTH}	5	20	ns	*2
$\overline{WE}$ Low to $\overline{WAIT}$ High		t_{WLTH}	0	20	ns	*2
$\overline{CE1}$ High to $\overline{WAIT}$ High-Z		t_{CHTZ}	—	20	ns	*2
$\overline{WE}$ High to $\overline{WAIT}$ High-Z		t_{WHTZ}	—	20	ns	*2
Burst End $\overline{CE1}$ Low Hold Time from CLK		t_{CKCLH}	5	—	ns	
Burst End $\overline{CE1}$ High Setup Time to next CLK		t_{CHCK}	5	—	ns	
Burst End $\overline{LB}$, $\overline{UB}$ Hold Time from CLK		t_{CKBH}	5	—	ns	
Burst Write Recovery Time		t_{WRB}	30	—	ns	*3
Burst Terminate Recovery Time	BL = 8, 16	t_{TRB}	30	—	ns	*4
	BL = Continuous		70	—	ns	*4

*1: Defined from the valid input edge to the High to Low transition of either $\overline{ADV}$, $\overline{CE1}$, or $\overline{WE}$, whichever occurs last. And once $\overline{LB}$, $\overline{UB}$ are determined, $\overline{LB}$, $\overline{UB}$ must not be changed until the end of burst write.

*2: The output load 50 pF with 50 Ω termination to $V_{DD} \times 0.5$ V.

*3: Defined from the valid clock edge where last data-input being latched at the end of burst write to the High to Low transition of either $\overline{ADV}$ or $\overline{CE1}$ whichever occurs late for the next access.

*4: Defined from the Low to High transition of $\overline{CE1}$ to the High to Low transition of either $\overline{ADV}$ or $\overline{CE1}$ whichever occurs late for the next access.

(7) Power Down Parameters

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
CE2 Low Setup Time for Power Down Entry	t_{CSP}	20	—	ns	
CE2 Low Hold Time after Power Down Entry	t_{C2LP}	70	—	ns	
$\overline{CE}$1 High Hold Time following CE2 High after Power Down Exit [Sleep mode only]	t_{CHH}	300	—	µs	*1
$\overline{CE}$1 High Hold Time following CE2 High after Power Down Exit [not in Sleep mode]	t_{CHHP}	70	—	ns	*2
$\overline{CE}$1 High Setup Time following CE2 High after Power Down Exit	t_{CHS}	0	—	ns	*1

*1 : Applicable also to power-up.

*2 : Applicable when 4 M-bit and 8 M-bit Partial mode is set.

(8) Other Timing Parameters

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
$\overline{CE}$1 High to $\overline{OE}$ Invalid Time for Standby Entry	t_{CHOX}	10	—	ns	
$\overline{CE}$1 High to $\overline{WE}$ Invalid Time for Standby Entry	t_{CHWX}	10	—	ns	*1
CE2 Low Hold Time after Power-up	t_{C2LH}	50	—	µs	
$\overline{CE}$1 High Hold Time following CE2 High after Power-up	t_{CHH}	300	—	µs	
Input Transition Time (except for CLK)	t_T	1	25	ns	*2, *3

*1 : Some data might be written into any address location if t_{CHWX} (Min) is not satisfied.

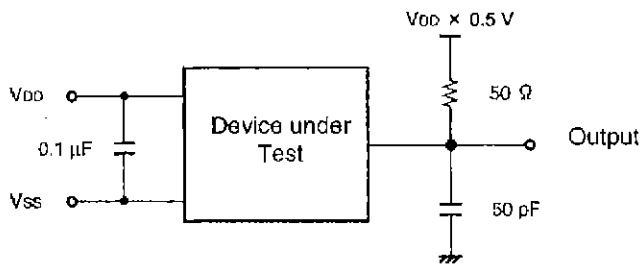
*2 : Except for clock input transition time.

*3 : The Input Transition Time (t_T) at AC testing is 5 ns for Asynchronous operation and 3 ns for Synchronous operation respectively. If actual t_T is longer than 5 ns or 3 ns specified as AC test condition, it may violate AC specification of some timing parameters. Refer to " (9) AC Test Conditions".

(9) AC Test Conditions

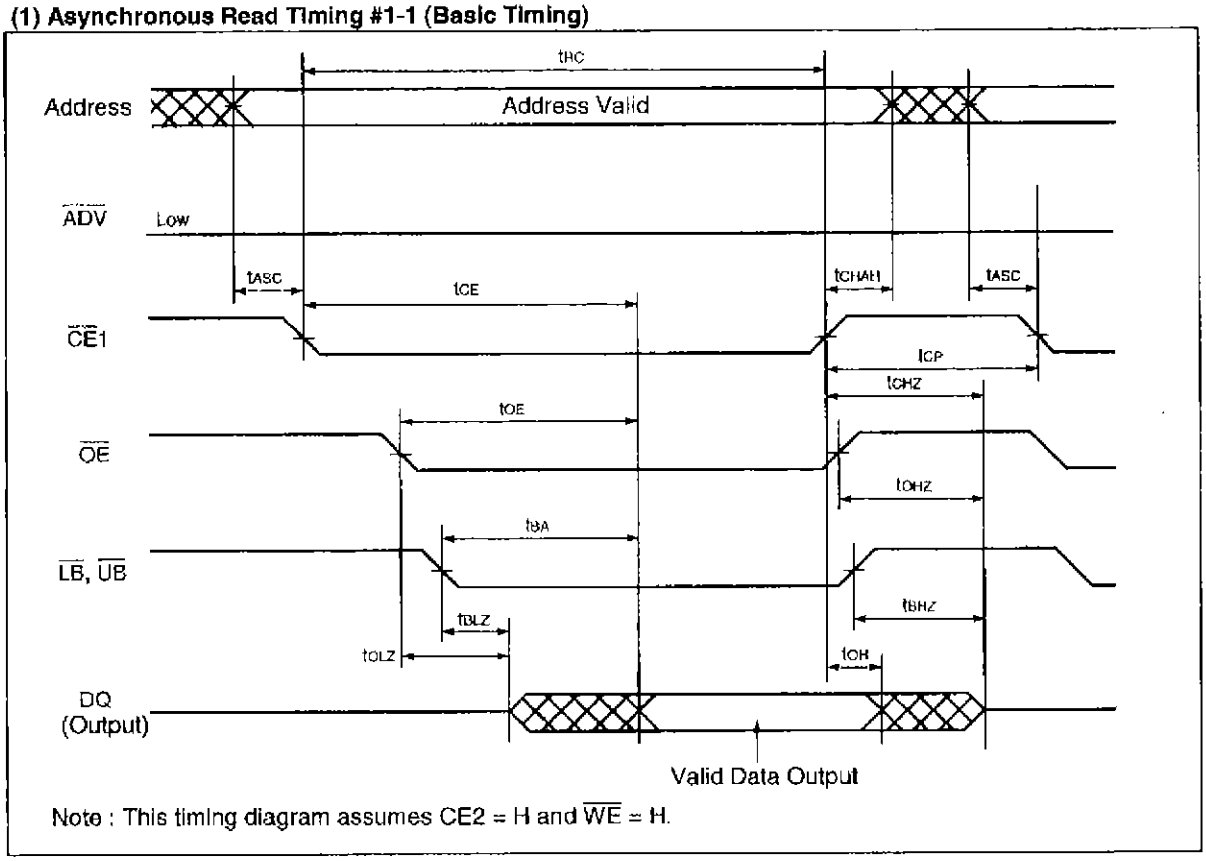
Description		Symbol	Test Setup	Value	Unit	Notes
Input High Level		V_{IH}	—	$V_{DD} \times 0.8$	V	
Input Low Level		V_{IL}	—	$V_{DD} \times 0.2$	V	
Input Timing Measurement Level		V_{REF}	—	$V_{DD} \times 0.5$	V	
Input Transition Time	Async.	t_T	Between V_{IL} and V_{IH}	5	ns	
	Sync.			3	ns	

• AC MEASUREMENT OUTPUT LOAD CIRCUIT



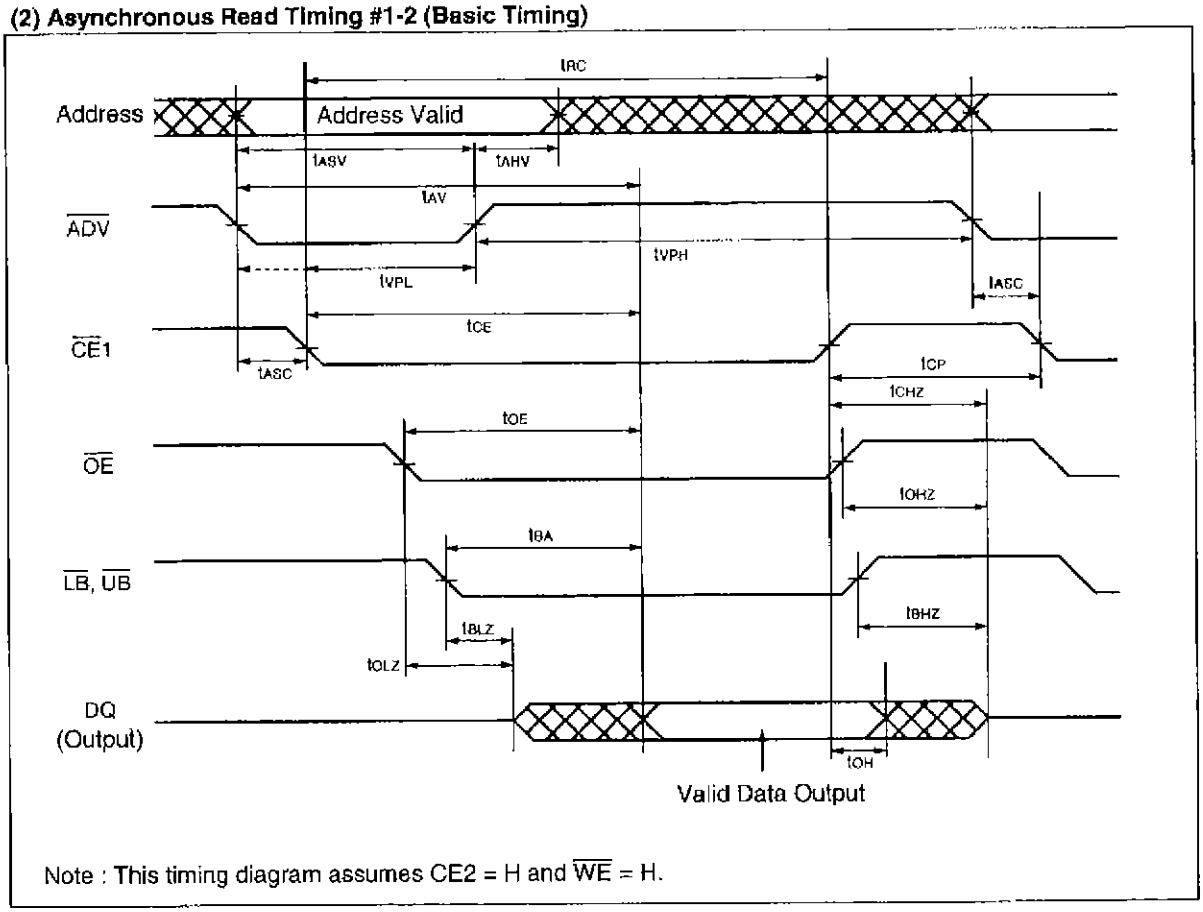
■ TIMING DIAGRAMS

(1) Asynchronous Read Timing #1-1 (Basic Timing)



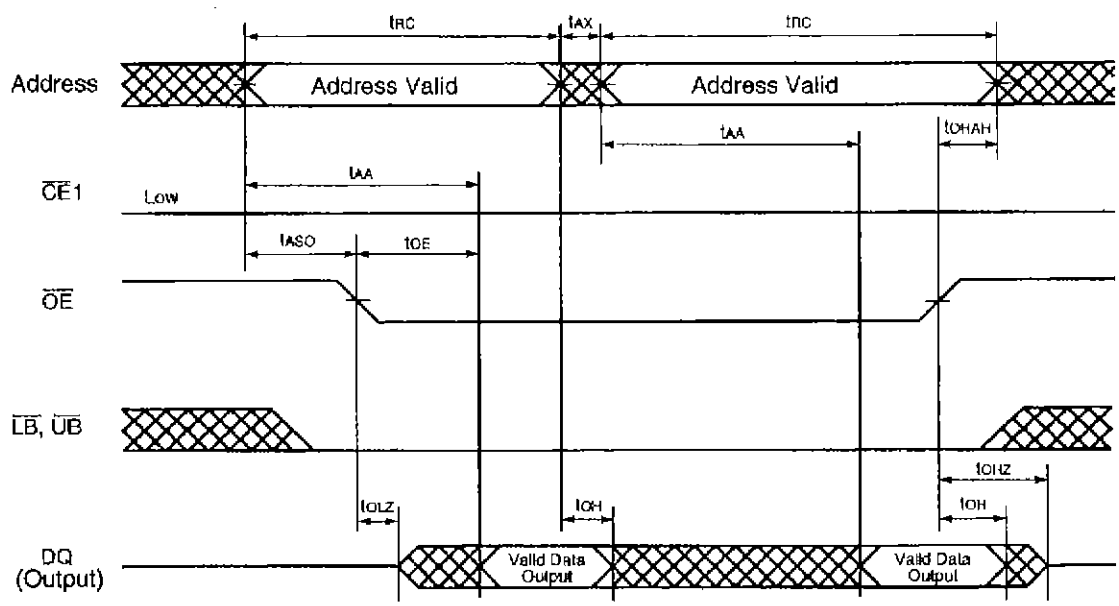
Note : This timing diagram assumes CE2 = H and $\overline{WE}$ = H.

(2) Asynchronous Read Timing #1-2 (Basic Timing)



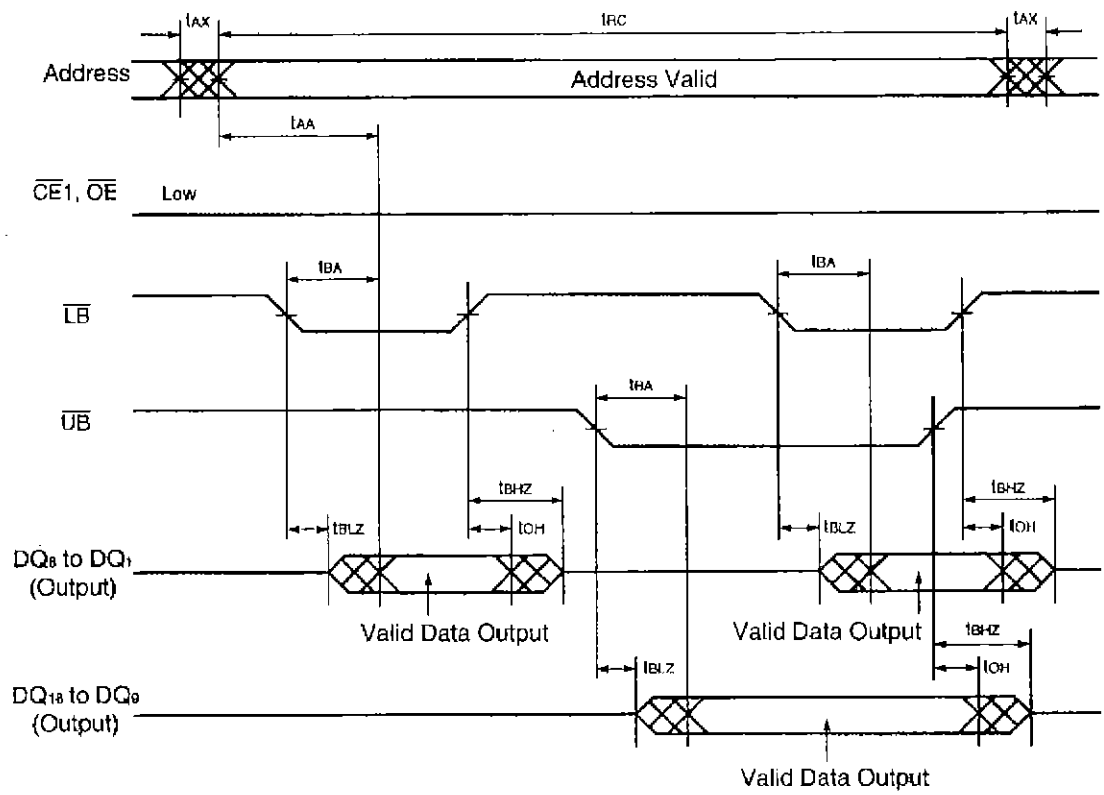
Note : This timing diagram assumes CE2 = H and $\overline{WE}$ = H.

(3) Asynchronous Read Timing #2 ($\overline{OE}$ Control & Address Access)



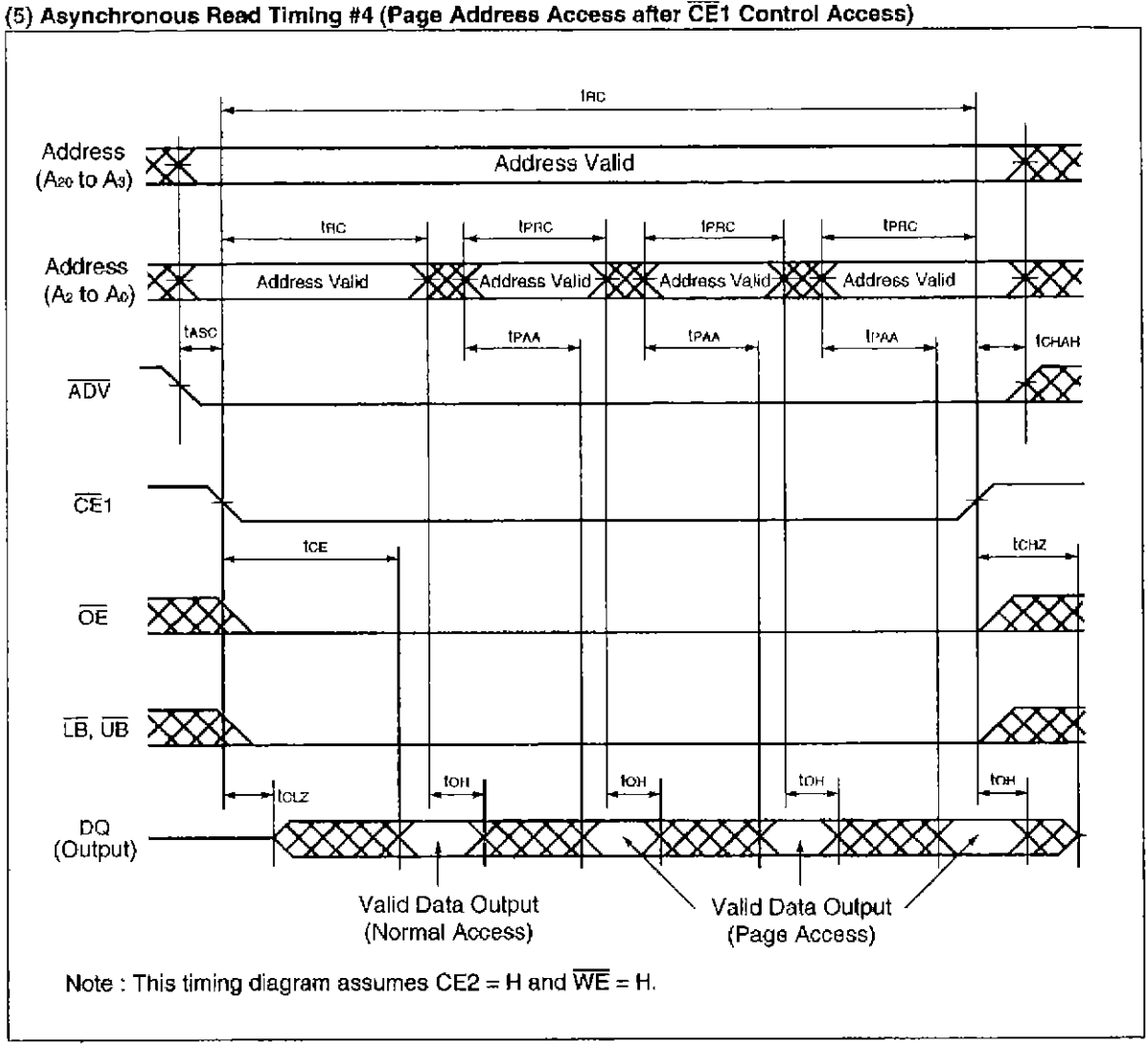
Note : This timing diagram assumes CE2 = H, $\overline{ADV}$ = L and $\overline{WE}$ = H.

(4) Asynchronous Read Timing #3 ($\overline{LB}$, $\overline{UB}$ Byte Control Access)



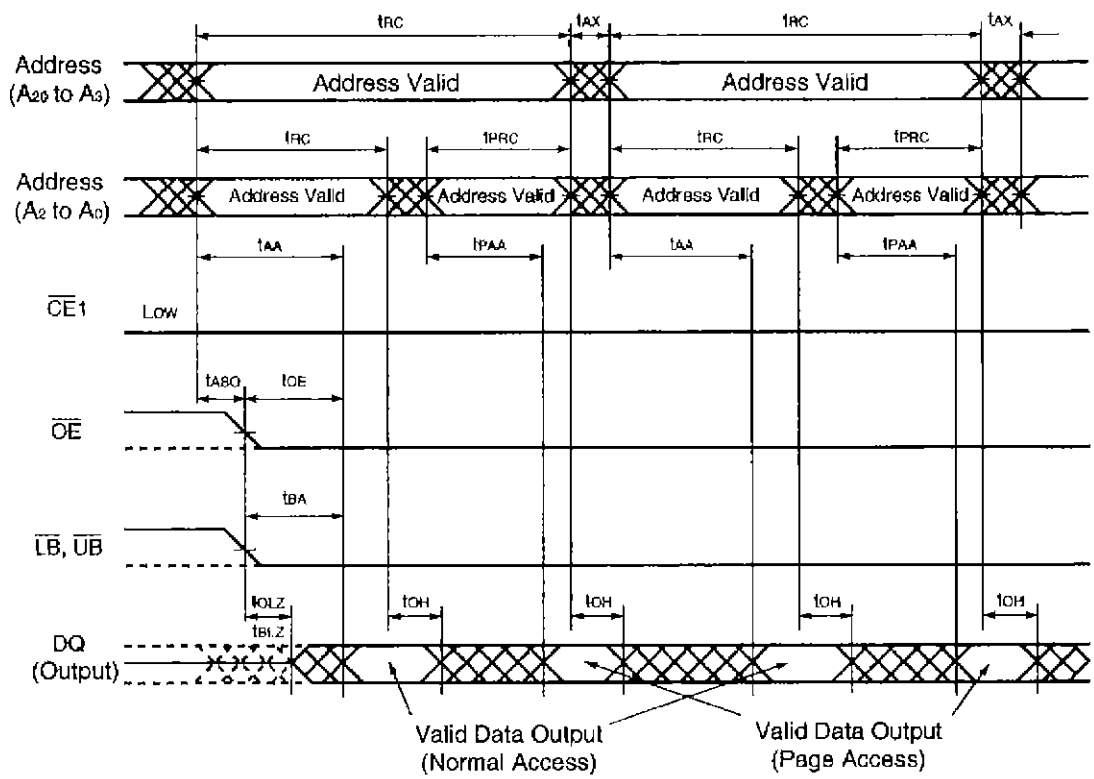
Note : This timing diagram assumes CE2 = H, $\overline{ADV}$ = L and $\overline{WE}$ = H.

(5) **Asynchronous Read Timing #4 (Page Address Access after $\overline{CE1}$ Control Access)**



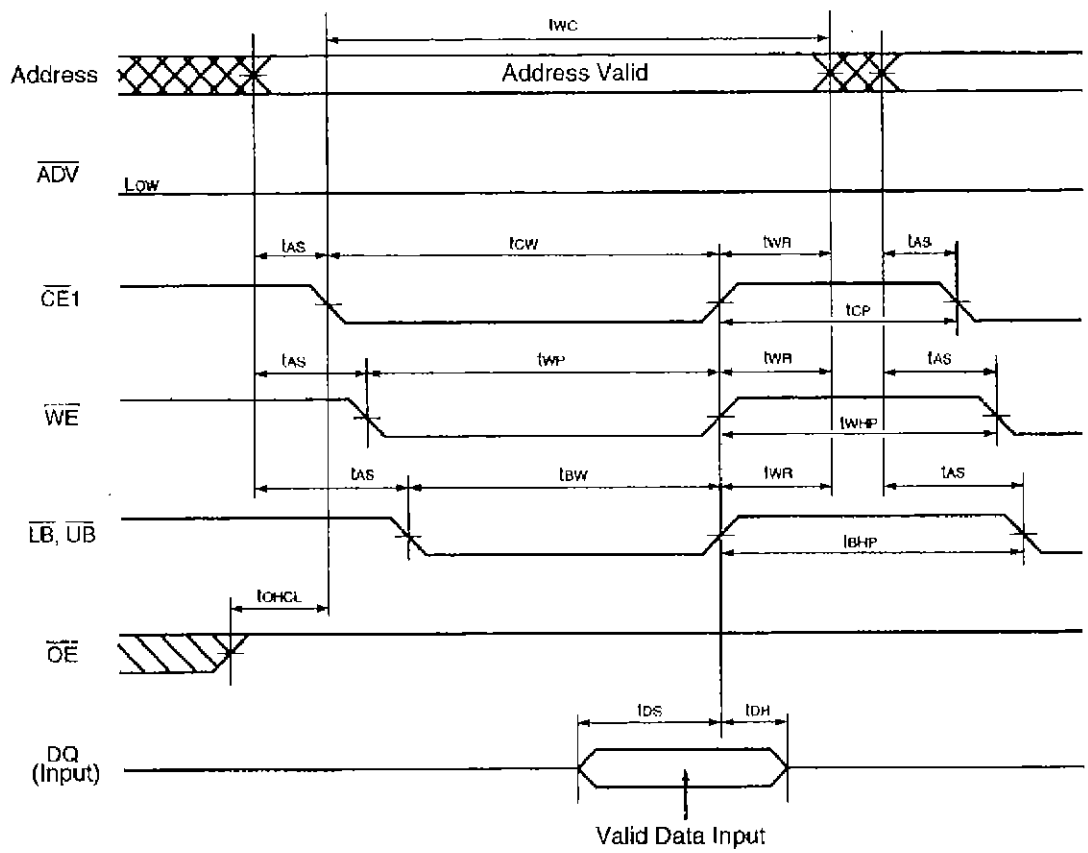
Note : This timing diagram assumes CE2 = H and $\overline{WE}$ = H.

(5) **Asynchronous Read Timing #5 (Random and Page Address Access)**



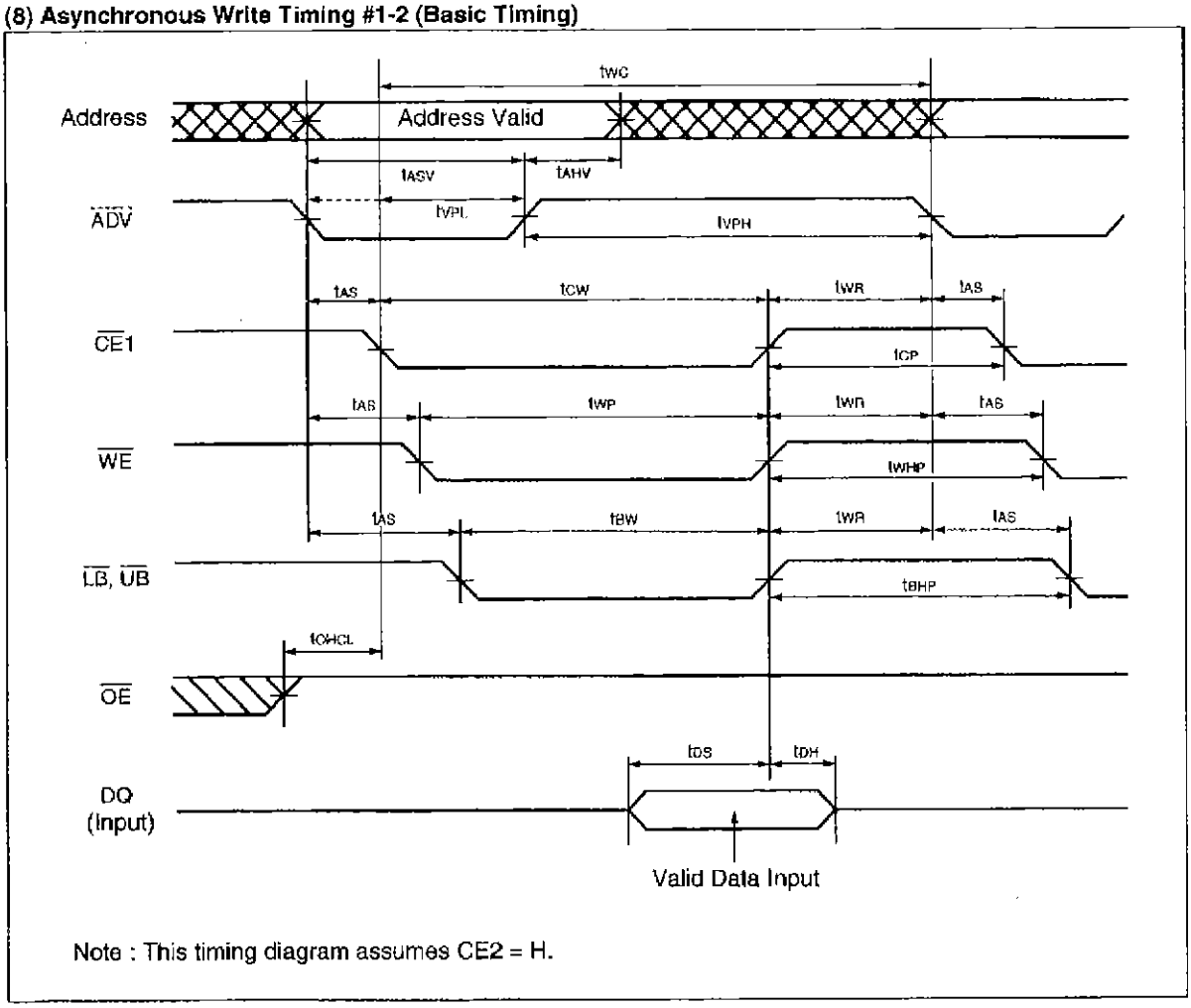
Notes : • This timing diagram assumes CE2 = H, $\overline{ADV}$ = L and $\overline{WE}$ = H.
• Either or both $\overline{LB}$ and $\overline{UB}$ must be Low when both $\overline{CE1}$ and $\overline{OE}$ are Low.

(7) Asynchronous Write Timing #1-1 (Basic Timing)



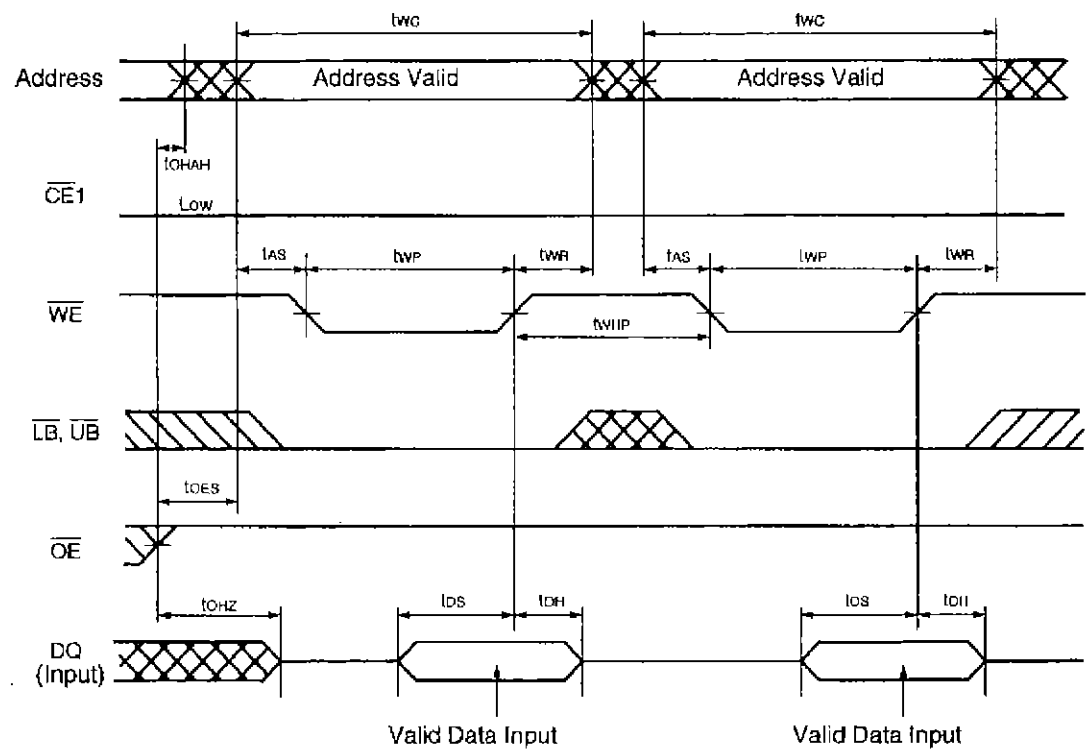
Note : This timing diagram assumes CE2 = H.

(8) Asynchronous Write Timing #1-2 (Basic Timing)



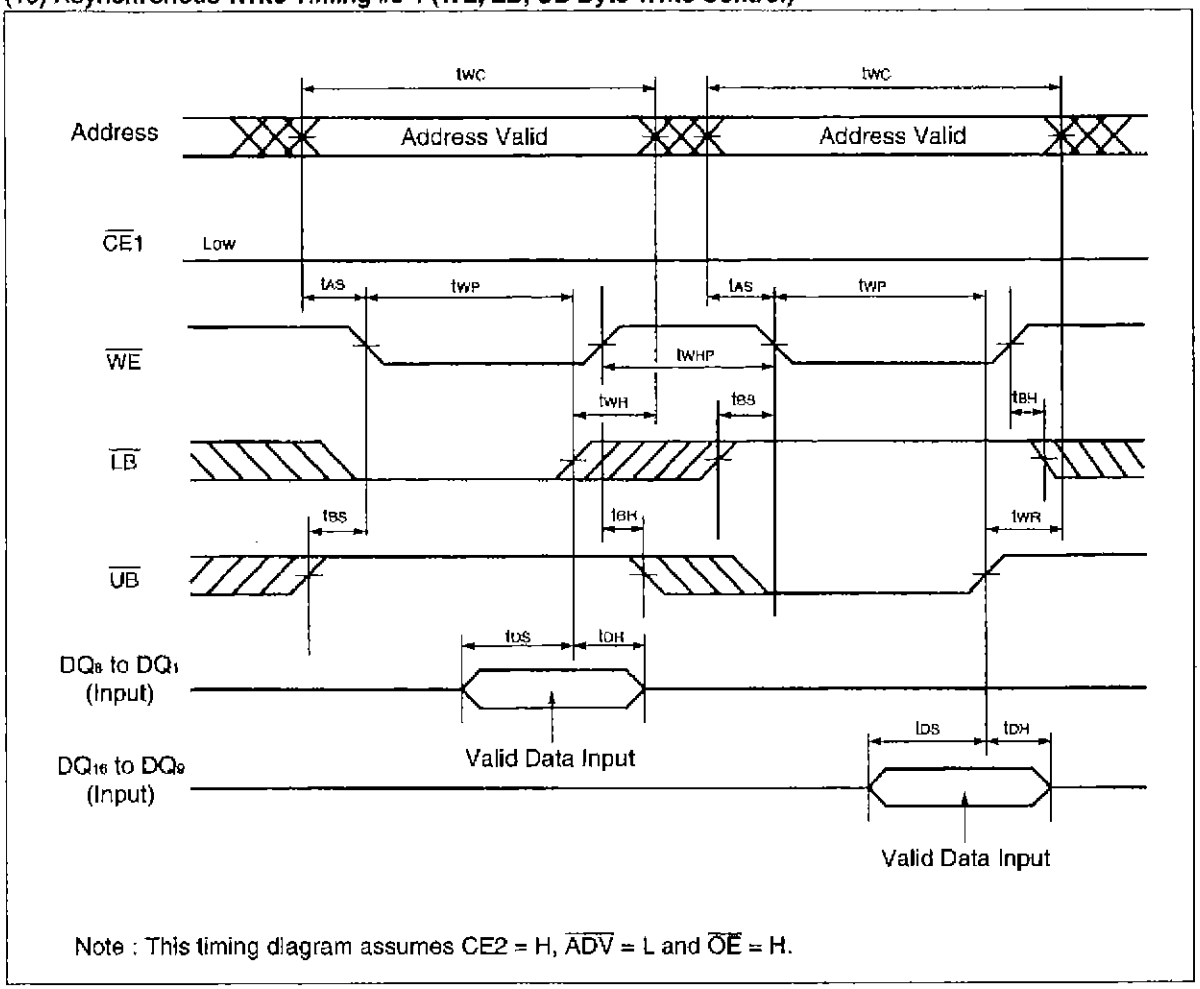
Note : This timing diagram assumes CE2 = H.

(9) **Asynchronous Write Timing #2 ($\overline{WE}$ Control)**



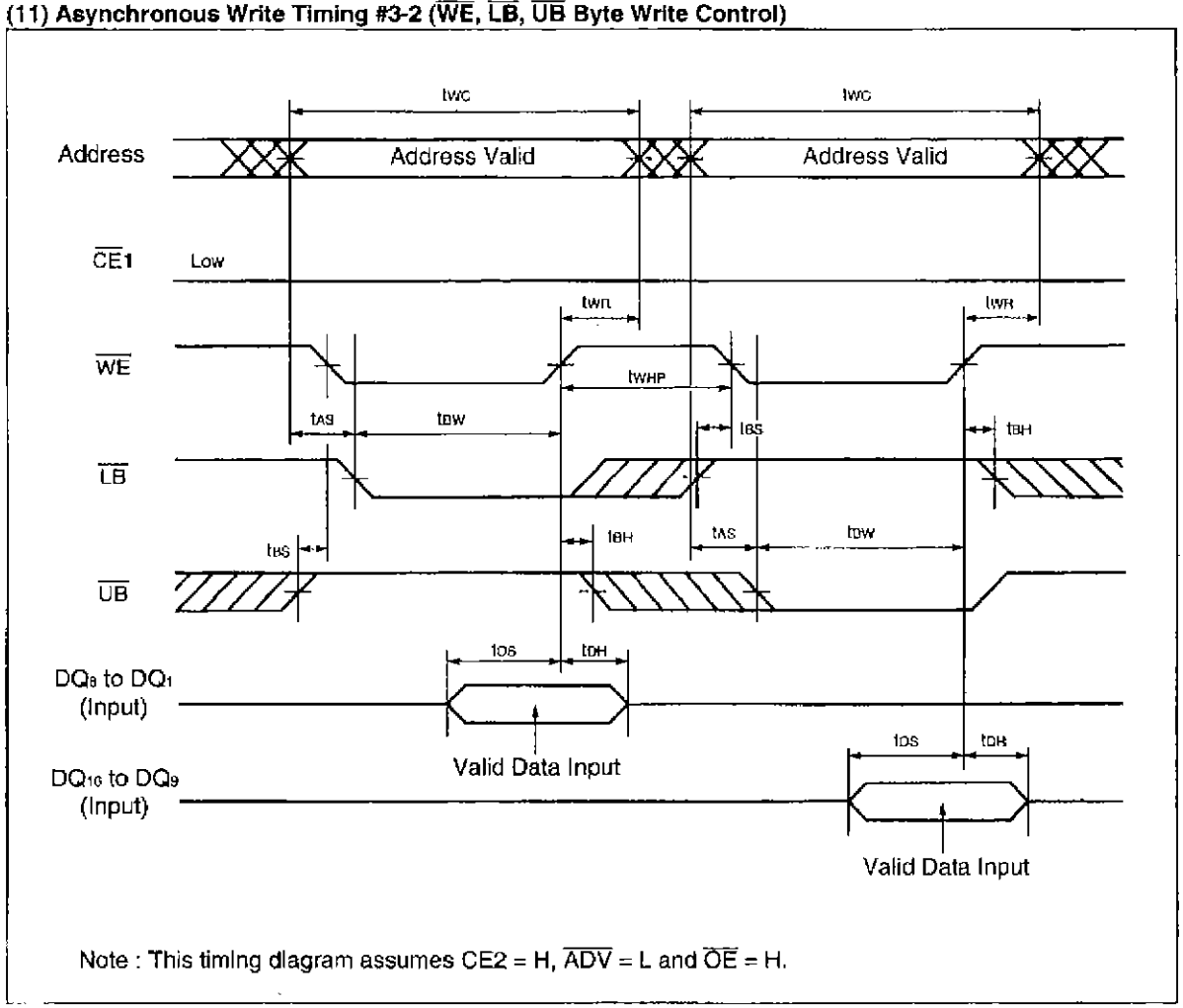
Note : This timing diagram assumes CE2 = H and $\overline{ADV}$ = L.

(10) Asynchronous Write Timing #3-1 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



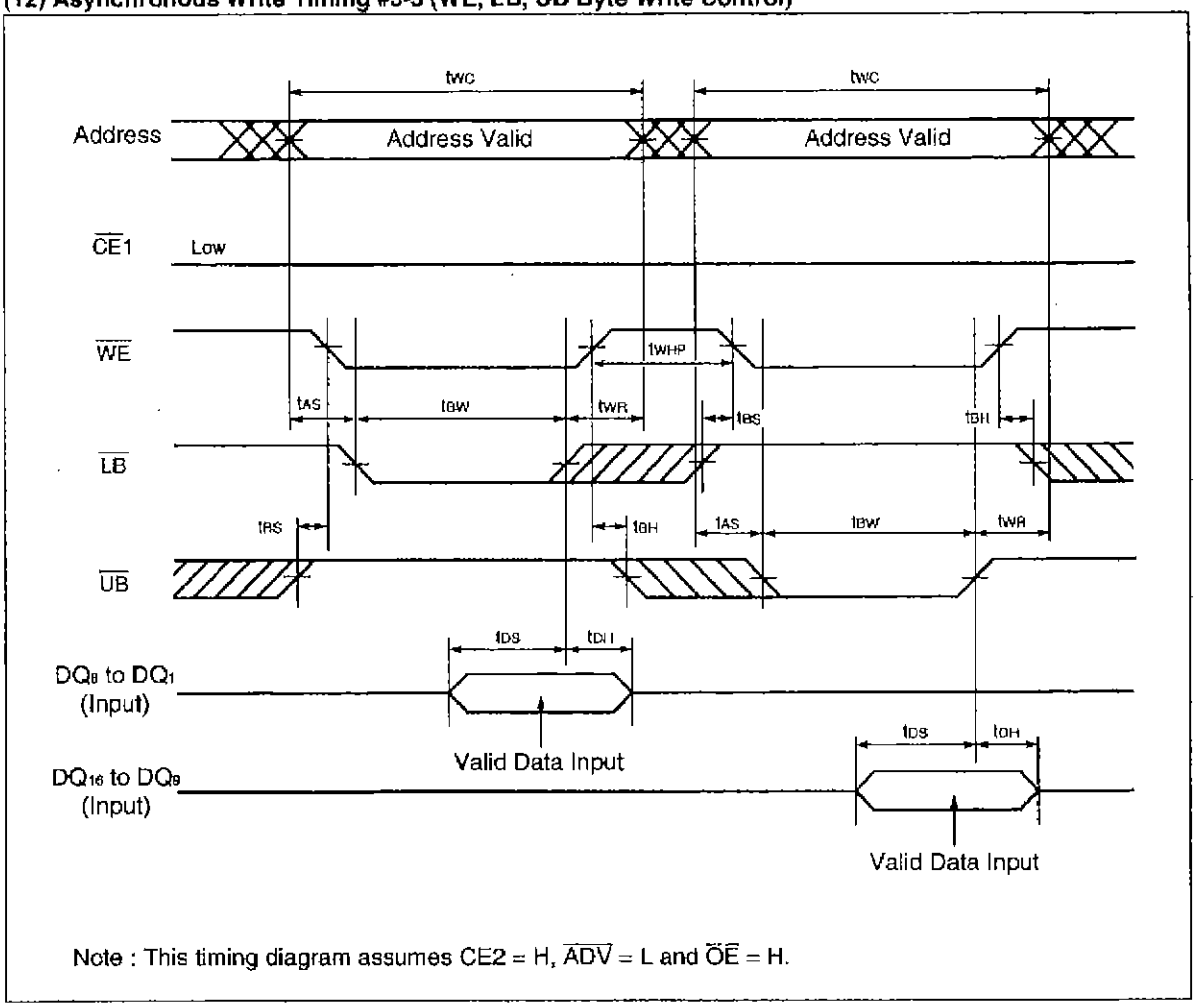
Note : This timing diagram assumes CE2 = H, $\overline{ADV}$ = L and $\overline{OE}$ = H.

(11) Asynchronous Write Timing #3-2 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



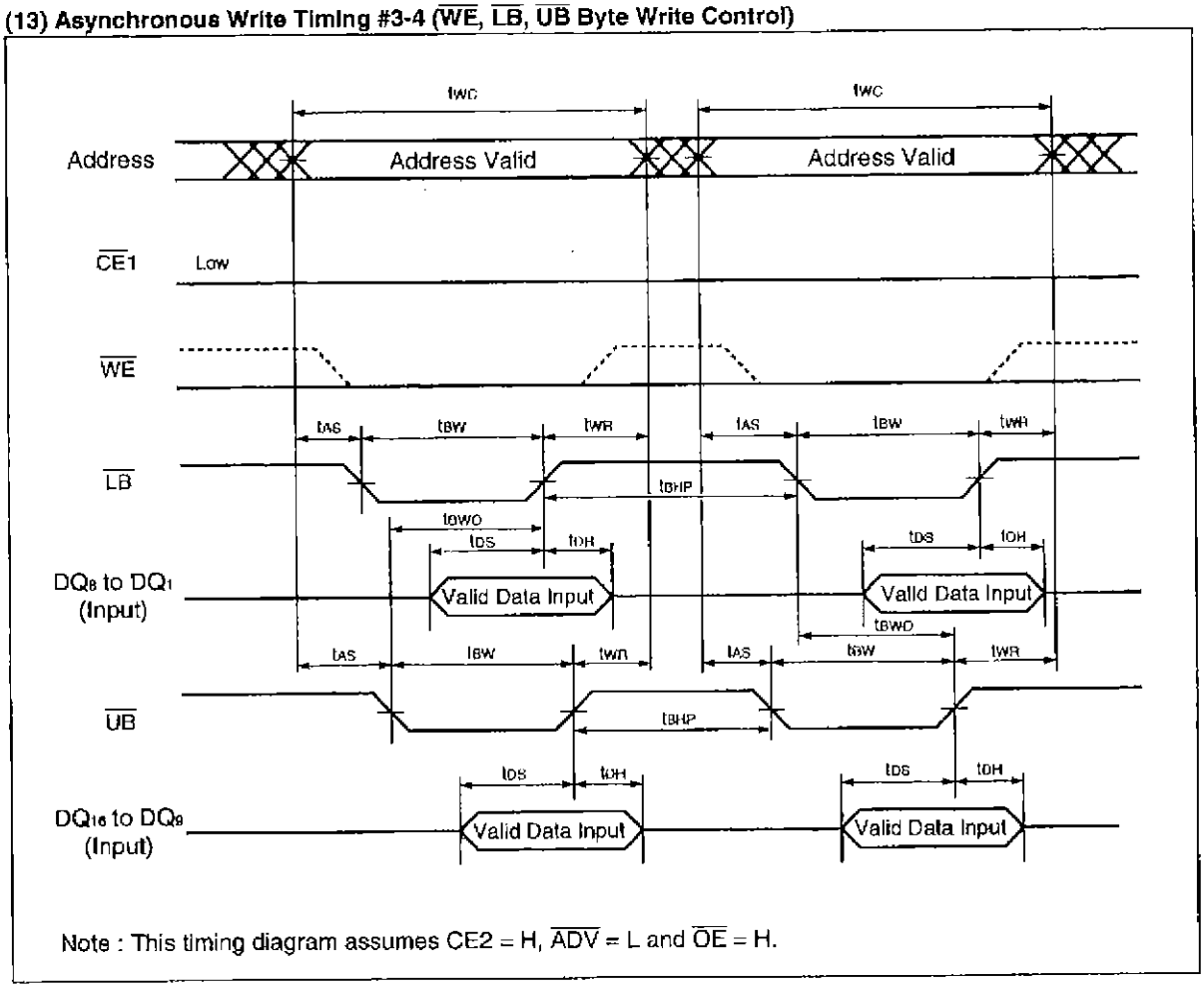
Note : This timing diagram assumes CE2 = H, $\overline{ADV}$ = L and $\overline{OE}$ = H.

(12) Asynchronous Write Timing #3-3 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



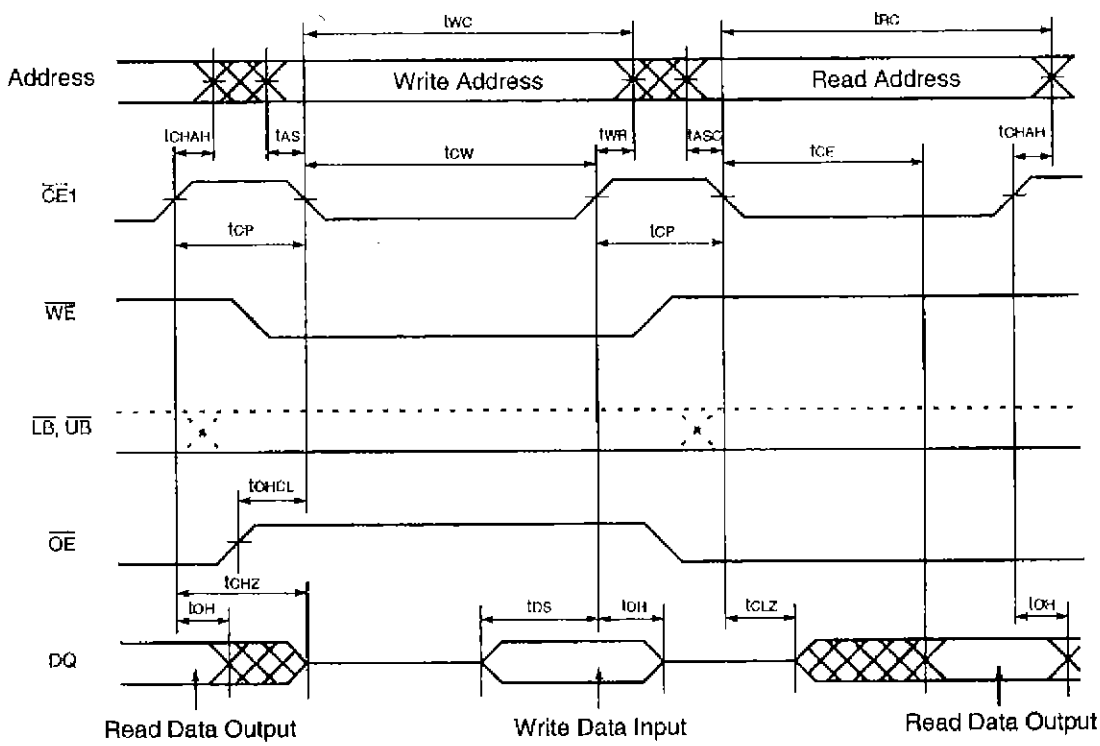
Note : This timing diagram assumes CE2 = H, $\overline{ADV}$ = L and $\overline{OE}$ = H.

(13) Asynchronous Write Timing #3-4 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



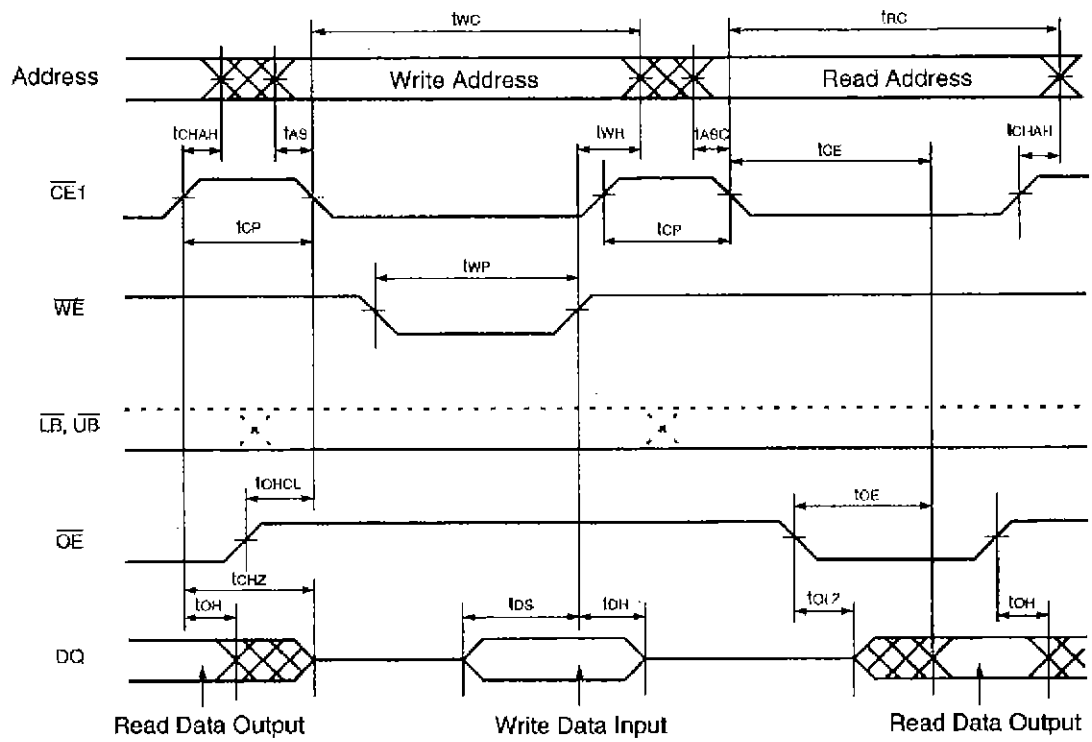
Note : This timing diagram assumes CE2 = H, $\overline{ADV}$ = L and $\overline{OE}$ = H.

(14) Asynchronous Read/Write Timing #1-1 ($\overline{CE}$1 Control)



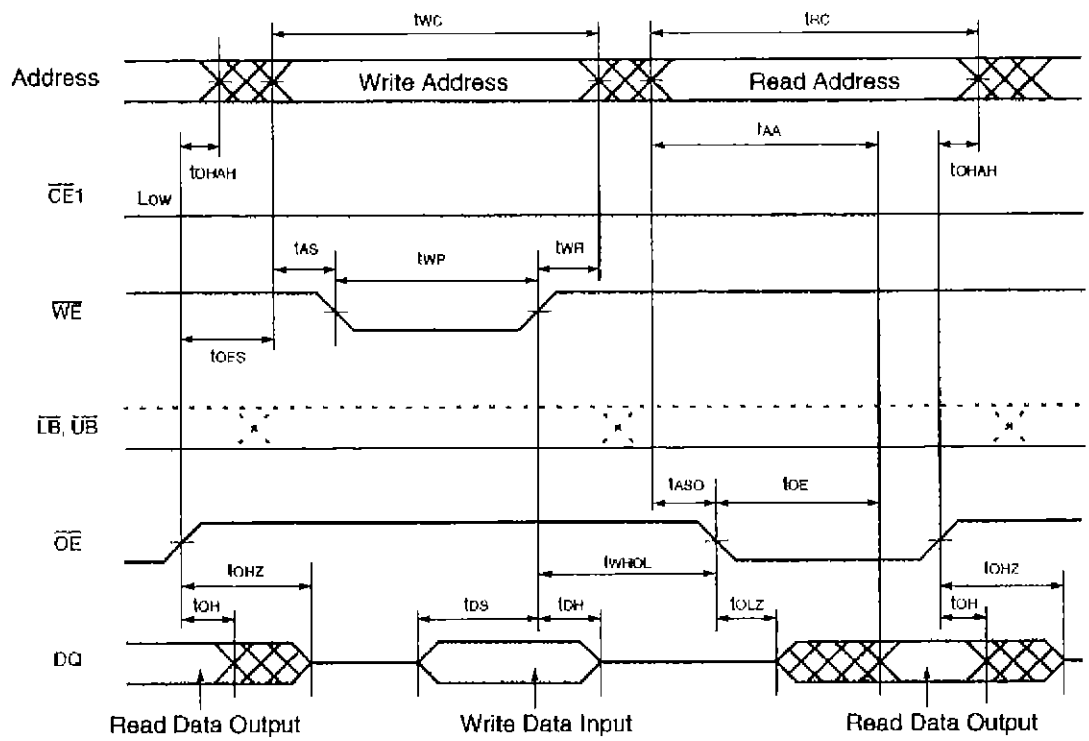
Notes : • This timing diagram assumes CE2 = H and $\overline{ADV}$ = L
• Write address is valid from either $\overline{CE}$1 or $\overline{WE}$ of last falling edge.

(15) Asynchronous Read/Write Timing #1-2 ($\overline{CE}$1, $\overline{WE}$, $\overline{OE}$ Control)



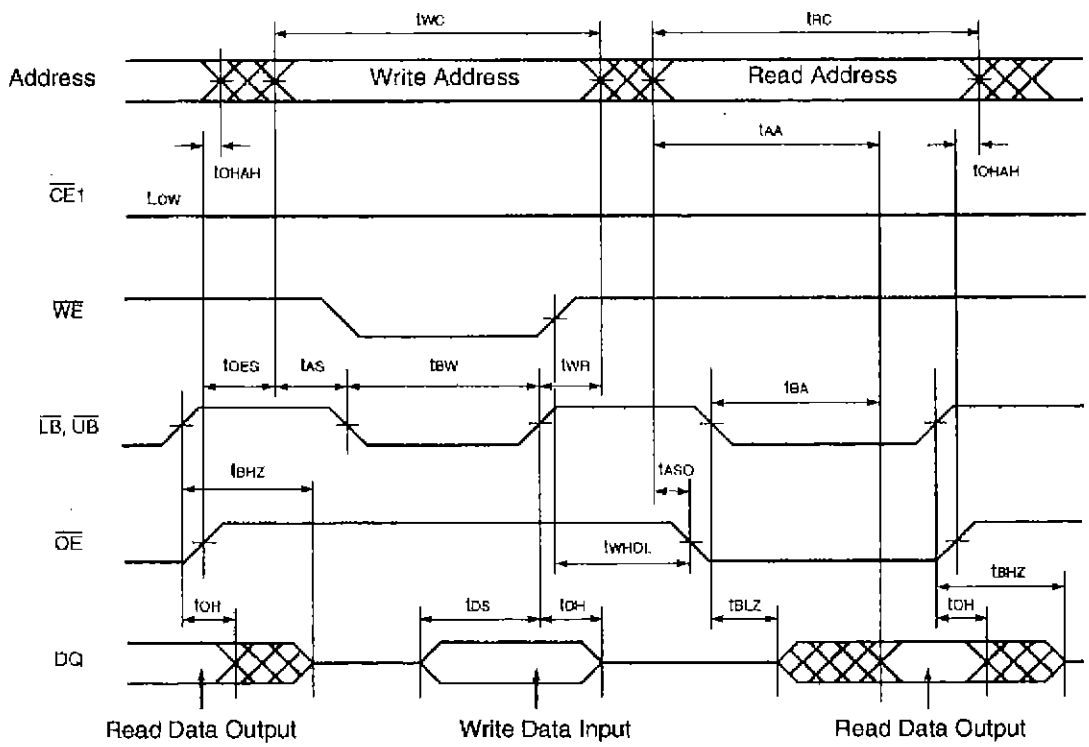
Notes : • This timing diagram assumes CE2 = H and $\overline{ADV}$ = L.
• $\overline{OE}$ can be fixed Low during write operation if it is $\overline{CE}$1 controlled write at Read-Write-Read sequence.

(16) Asynchronous Read/Write Timing #2 ($\overline{OE}$, $\overline{WE}$ Control)



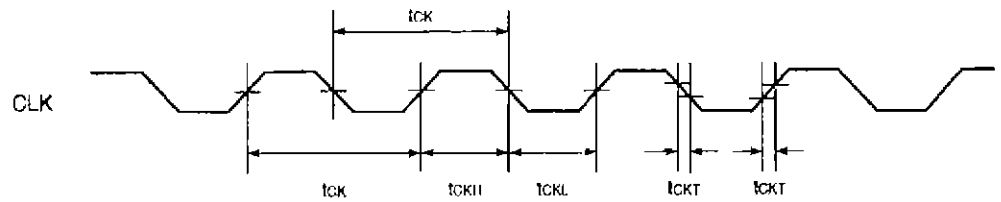
Notes : • This timing diagram assumes $\overline{CE2}$ = H and $\overline{ADV}$ = L.
• $\overline{CE1}$ can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.

(17) Asynchronous Read/Write Timing #3 ($\overline{OE}$, $\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Control)



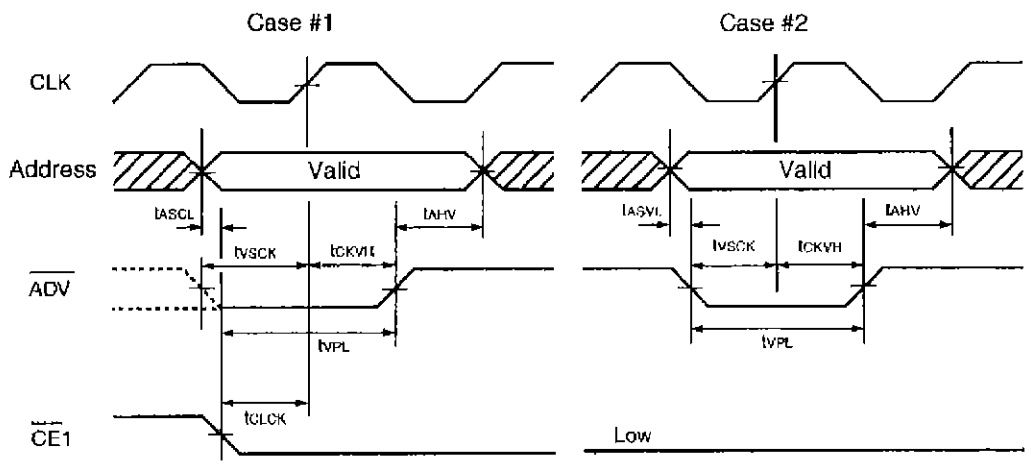
Notes : • This timing diagram assumes CE2 = H and $\overline{ADV}$ = L.
• $\overline{CE}$1 can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.

(18) Clock Input Timing



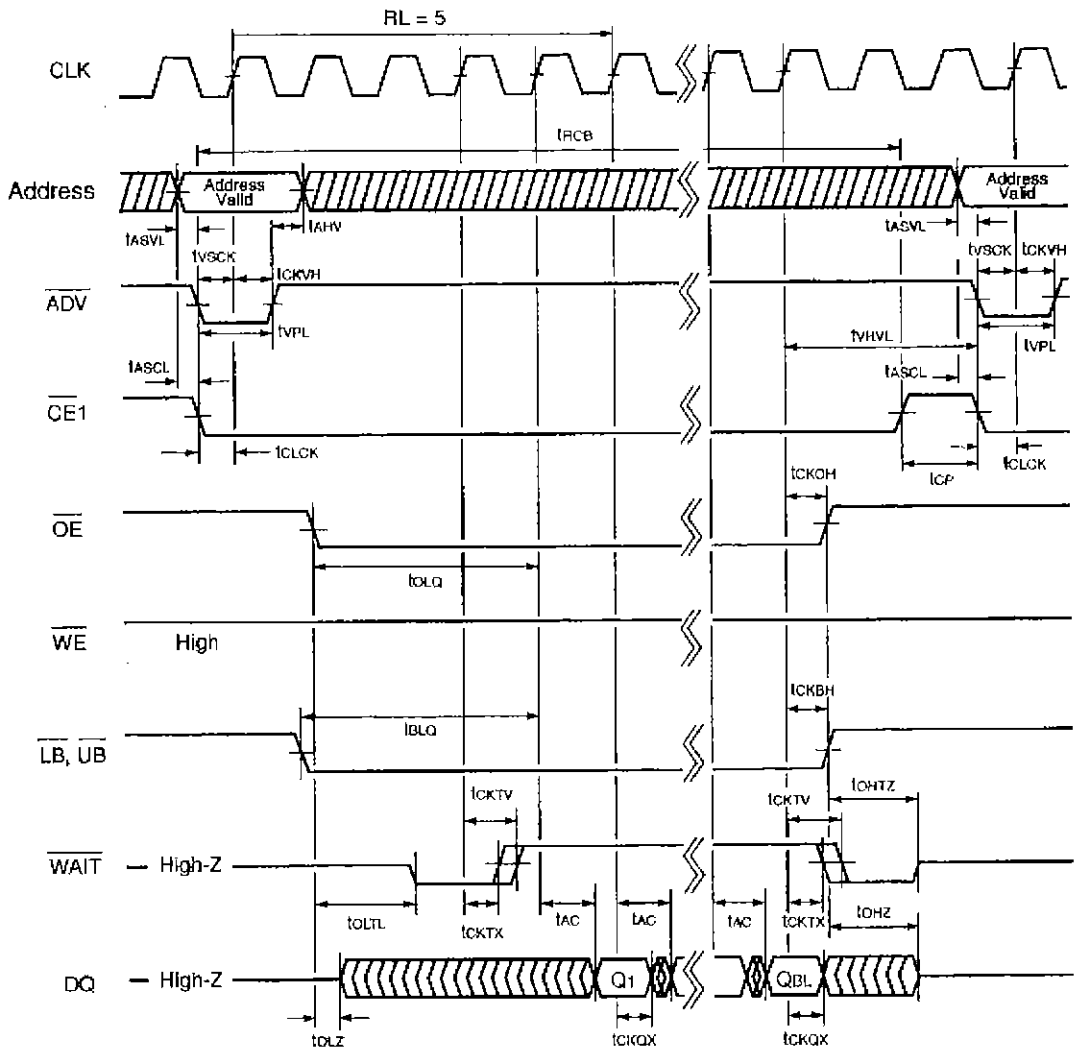
Notes : • Stable clock input must be required during $\overline{CE}1$ = L.
• t_{CK} is defined between valid clock edges.
• t_{CKT} is defined between V_{IH} (Min) and V_{IL} (Max)

(19) Address Latch Timing (Synchronous Mode)



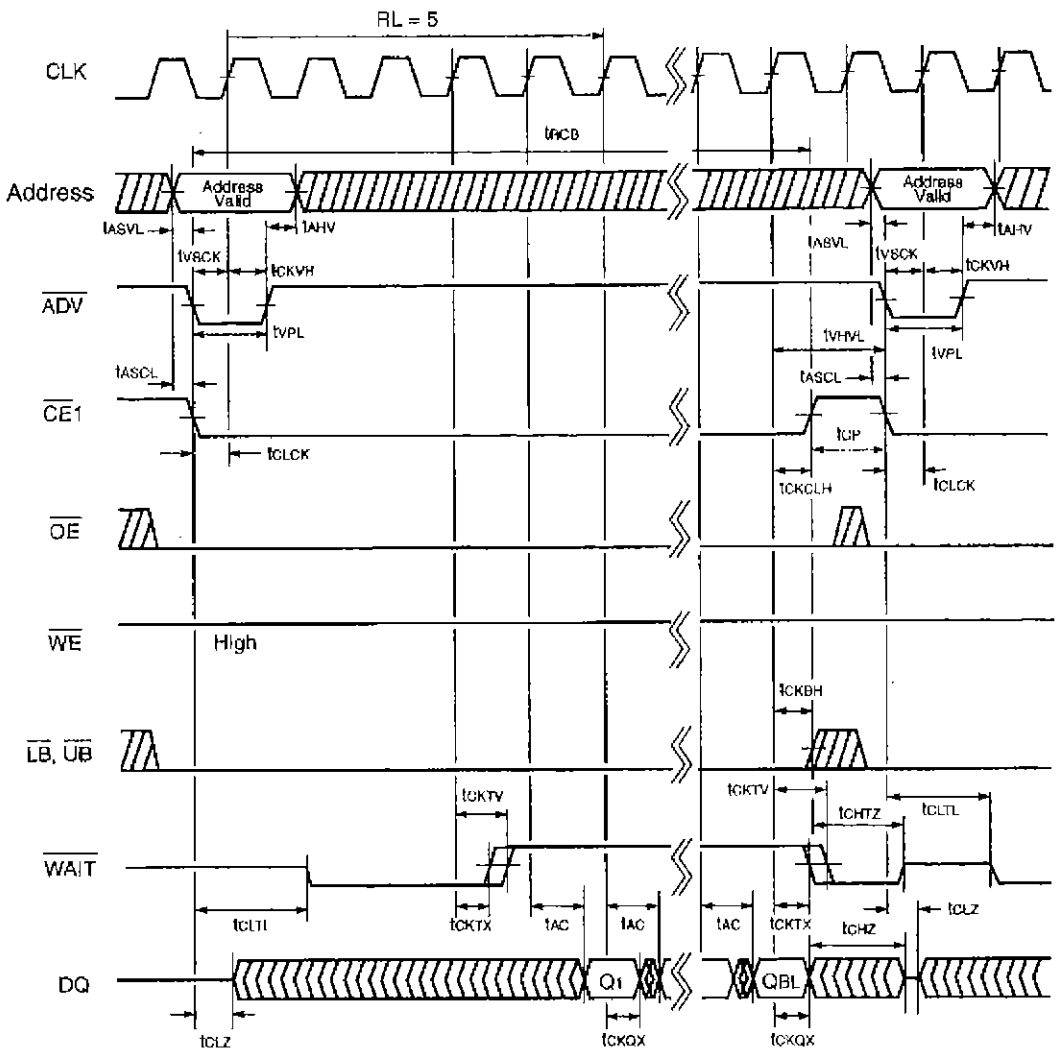
Notes : • Case #1 is the timing when $\overline{CE}1$ is brought to Low after $\overline{ADV}$ is brought to Low.
Case #2 is the timing when $\overline{ADV}$ is brought to Low after $\overline{CE}1$ is brought to Low.
• t_{VPL} is specified from the falling edge of either $\overline{CE}1$ or $\overline{ADV}$ whichever comes late.
At least one valid clock edge must be input during $\overline{ADV}$ = L.
• t_{VSCK} and t_{CLCK} are applied to the 1st valid clock edge during $\overline{ADV}$=L.

(20) Synchronous Read Timing #1 ($\overline{OE}$ Control)



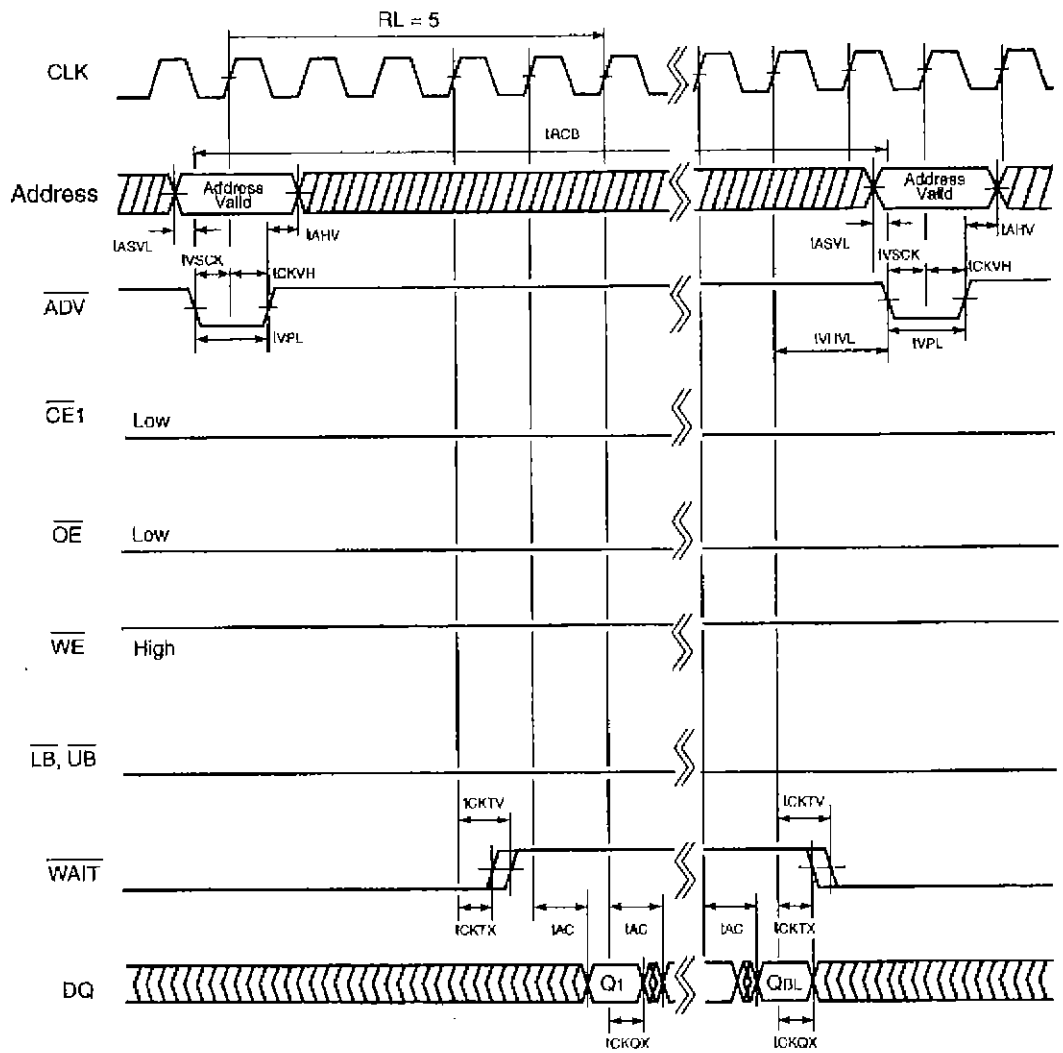
Note : This timing diagram assumes CE2 = H, the valid clock edge on rising edge and BL = 8 or 16.

(21) Synchronous Read Timing #2 ($\overline{CE1}$ Control)



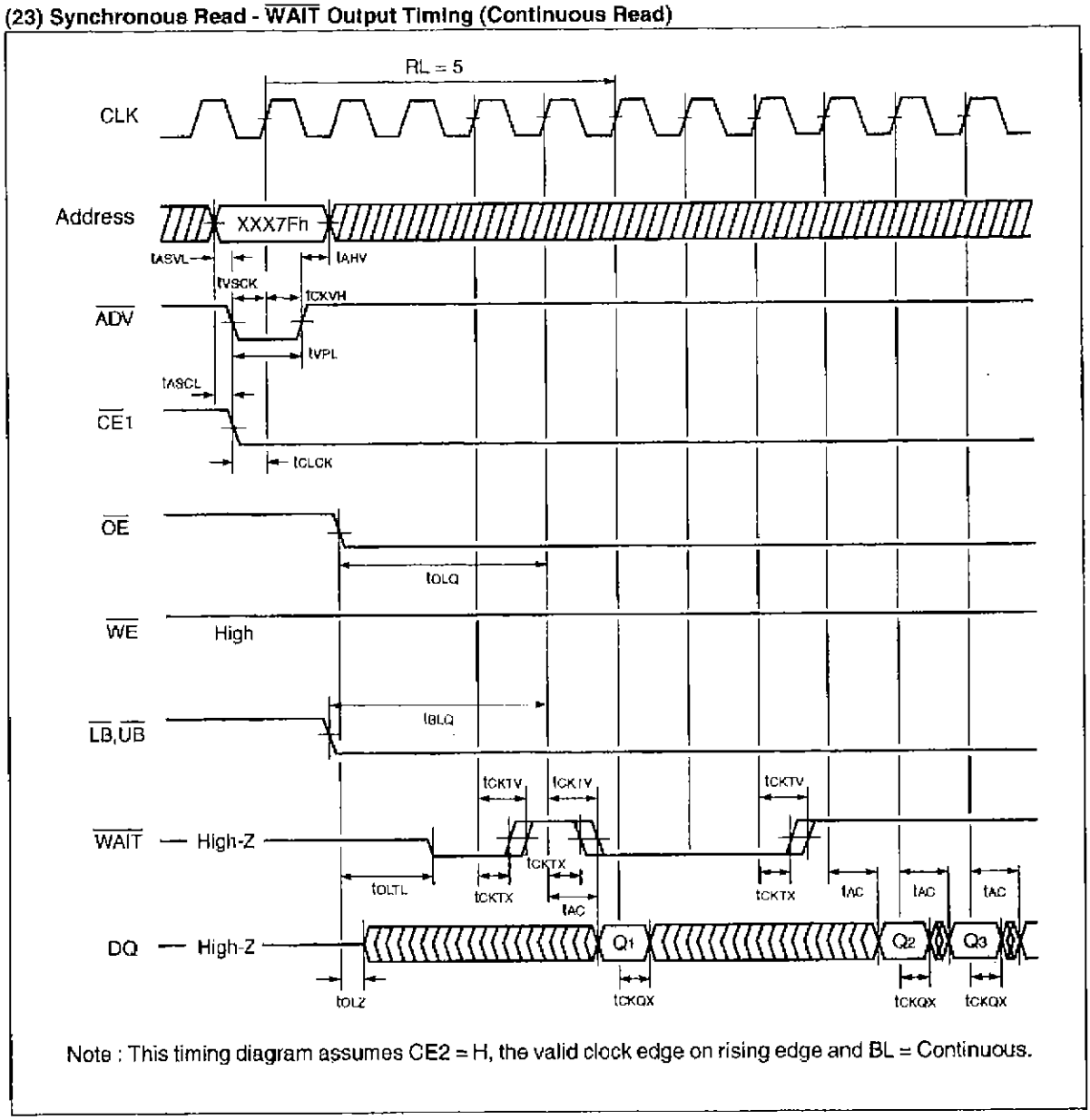
Note : This timing diagram assumes CE2 = H, the valid clock edge on rising edge and BL = 8 or 16.

(22) Synchronous Read Timing #3 ($\overline{ADV}$ Control)



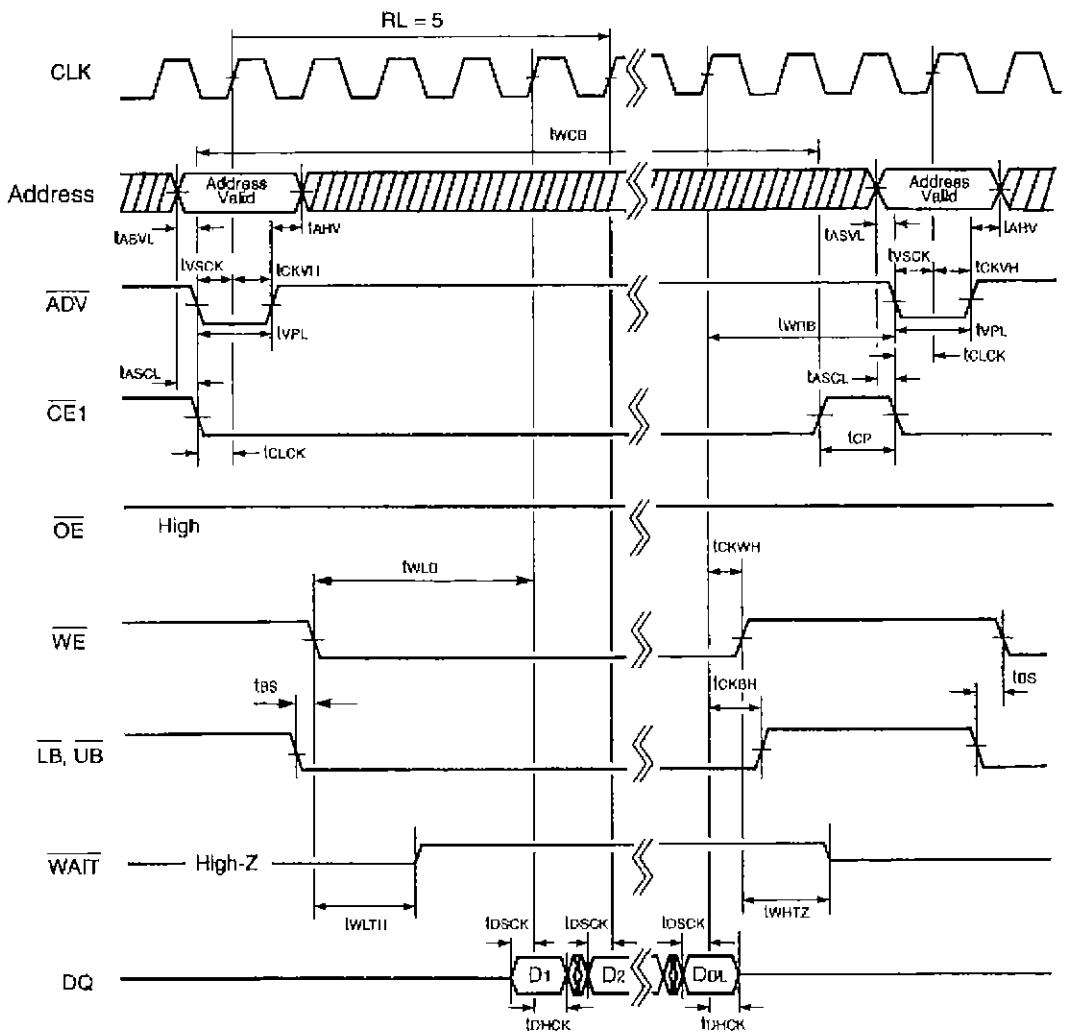
Note : This timing diagram assumes CE2 = H, the valid clock edge on rising edge and BL = 8 or 16.

(23) Synchronous Read - $\overline{\text{WAIT}}$ Output Timing (Continuous Read)



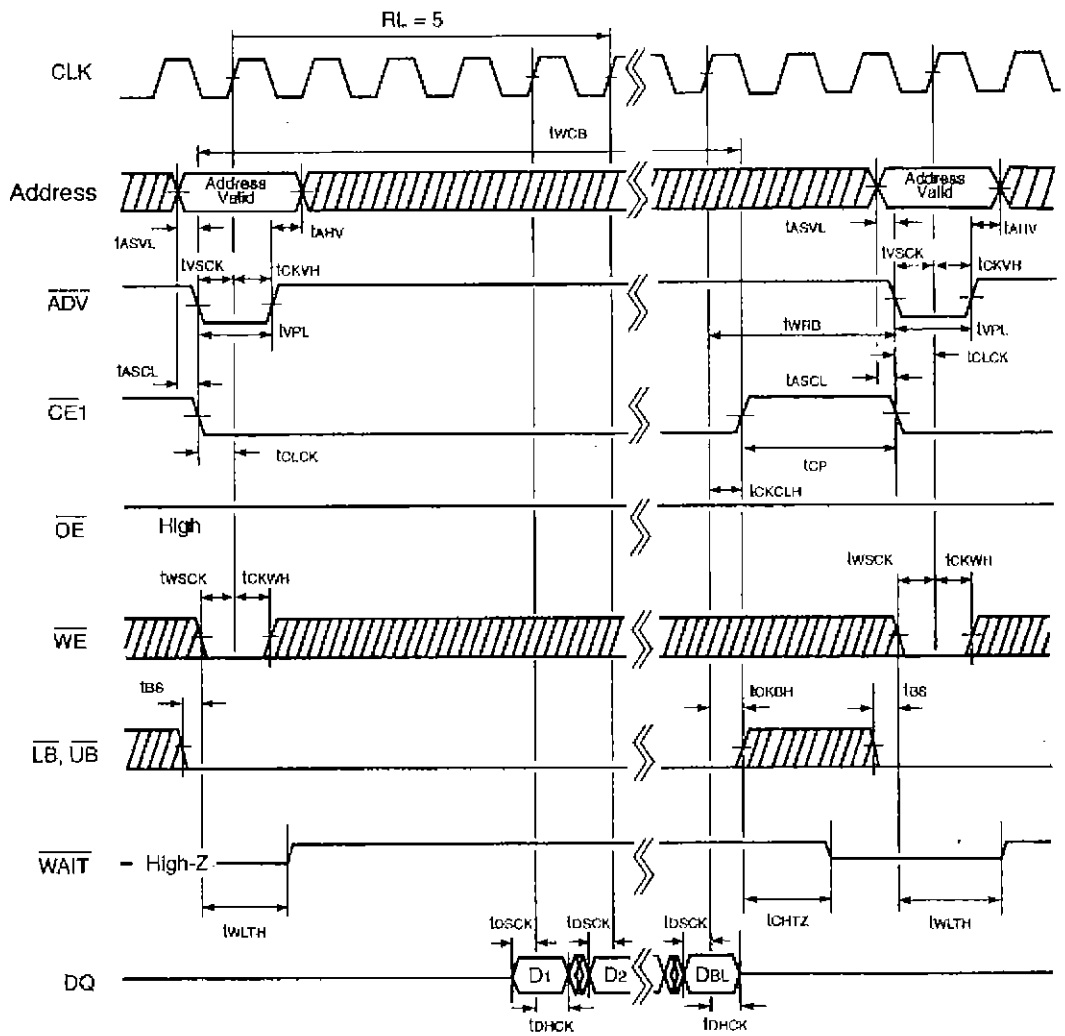
Note : This timing diagram assumes CE2 = H, the valid clock edge on rising edge and BL = Continuous.

(24) Synchronous Write Timing #1 ($\overline{WE}$ Level Control)



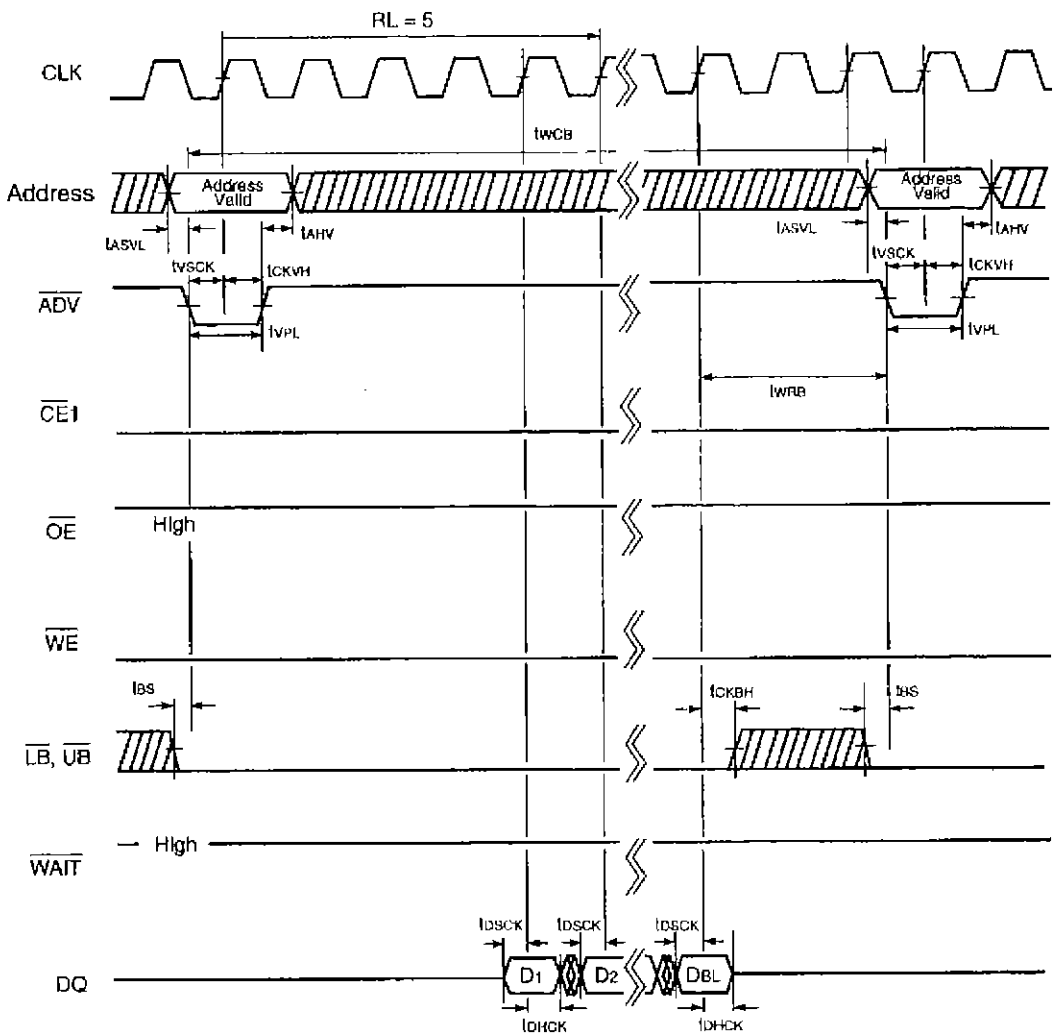
Note : This timing diagram assumes CE2 = H, the valid clock edge on rising edge and BL = 8 or 16.

(25) Synchronous Write Timing #2 ($\overline{WE}$ Single Clock Pulse Timing)



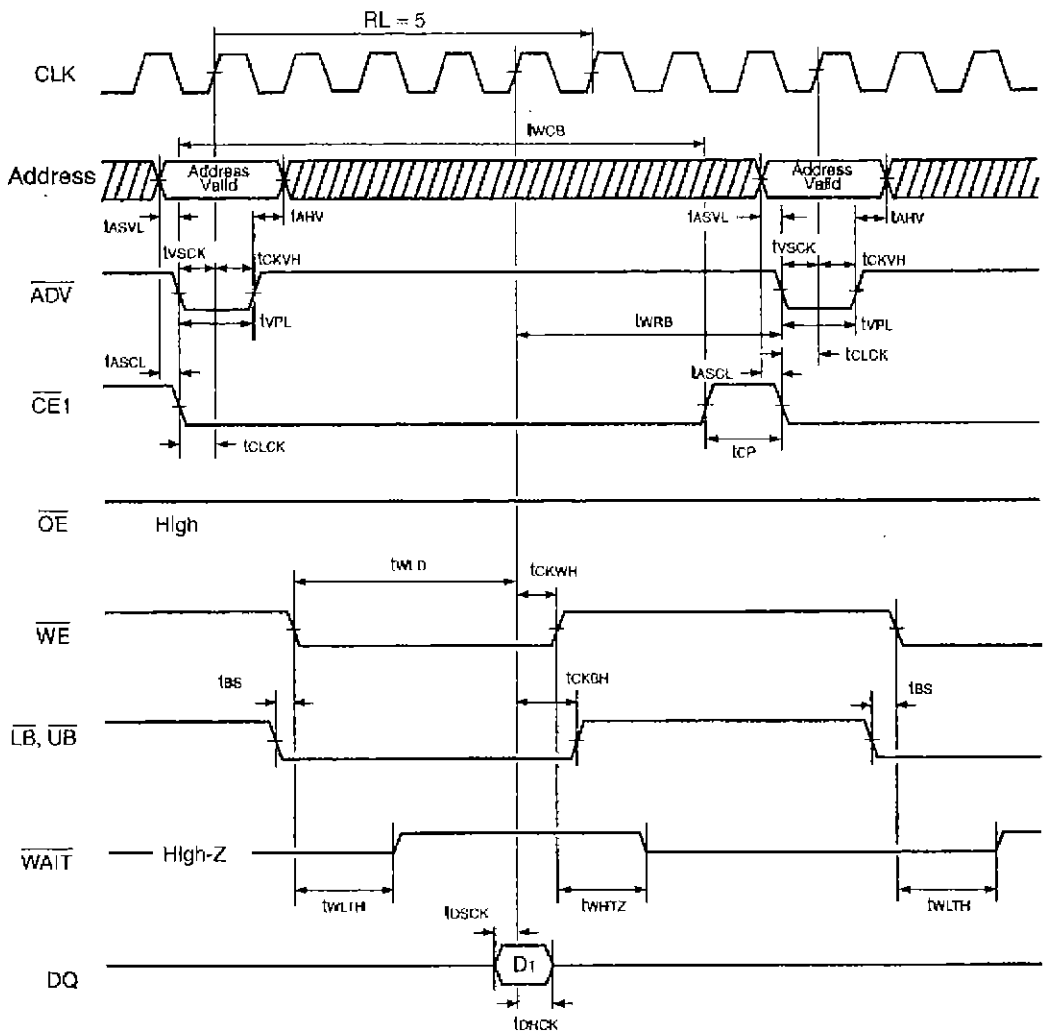
Note : This timing diagram assumes CE2 = H, the valid clock edge on rising edge and BL = 8 or 16.

(26) Synchronous Write Timing #3 ($\overline{ADV}$ Control)



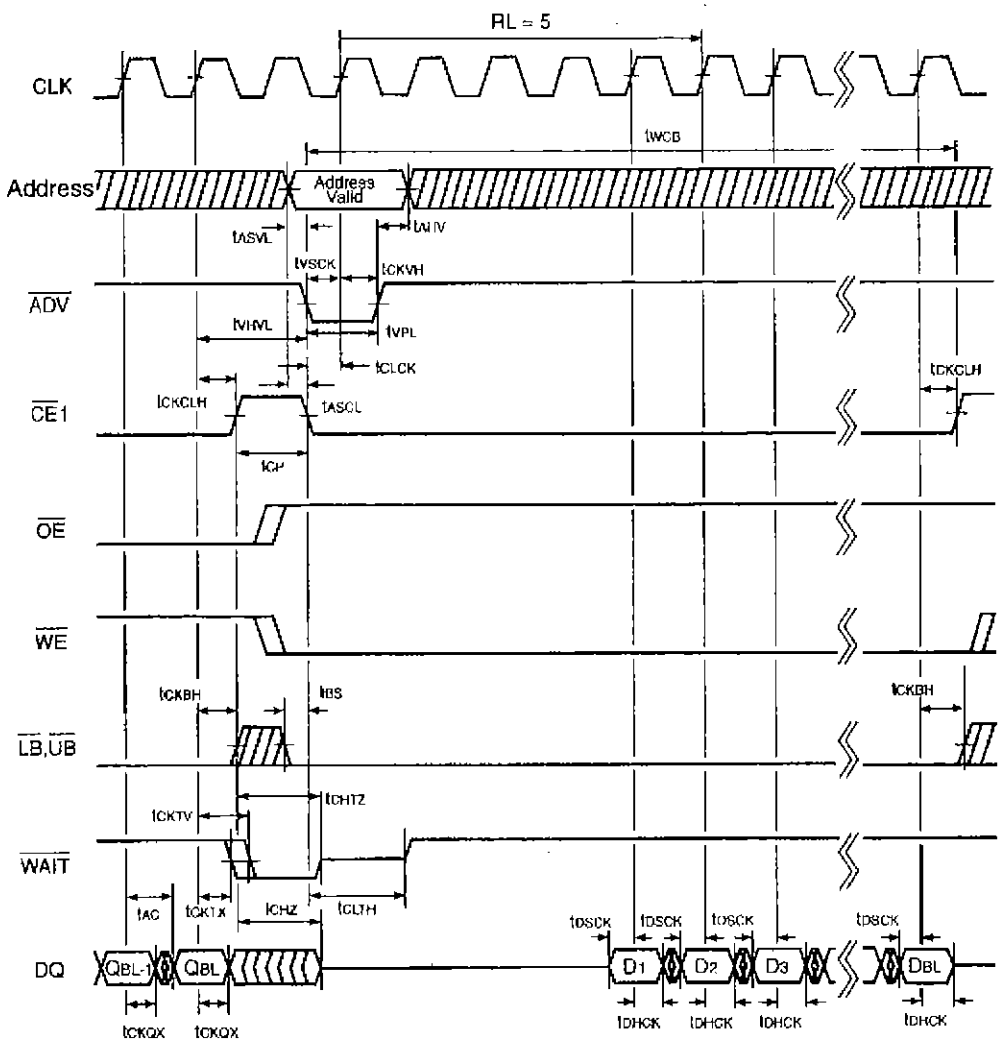
Note : This timing diagram assumes CE2 = H, the valid clock edge on rising edge and BL = 8 or 16.

(27) Synchronous Write Timing #4 ($\overline{WE}$ Level Control, Single Write)



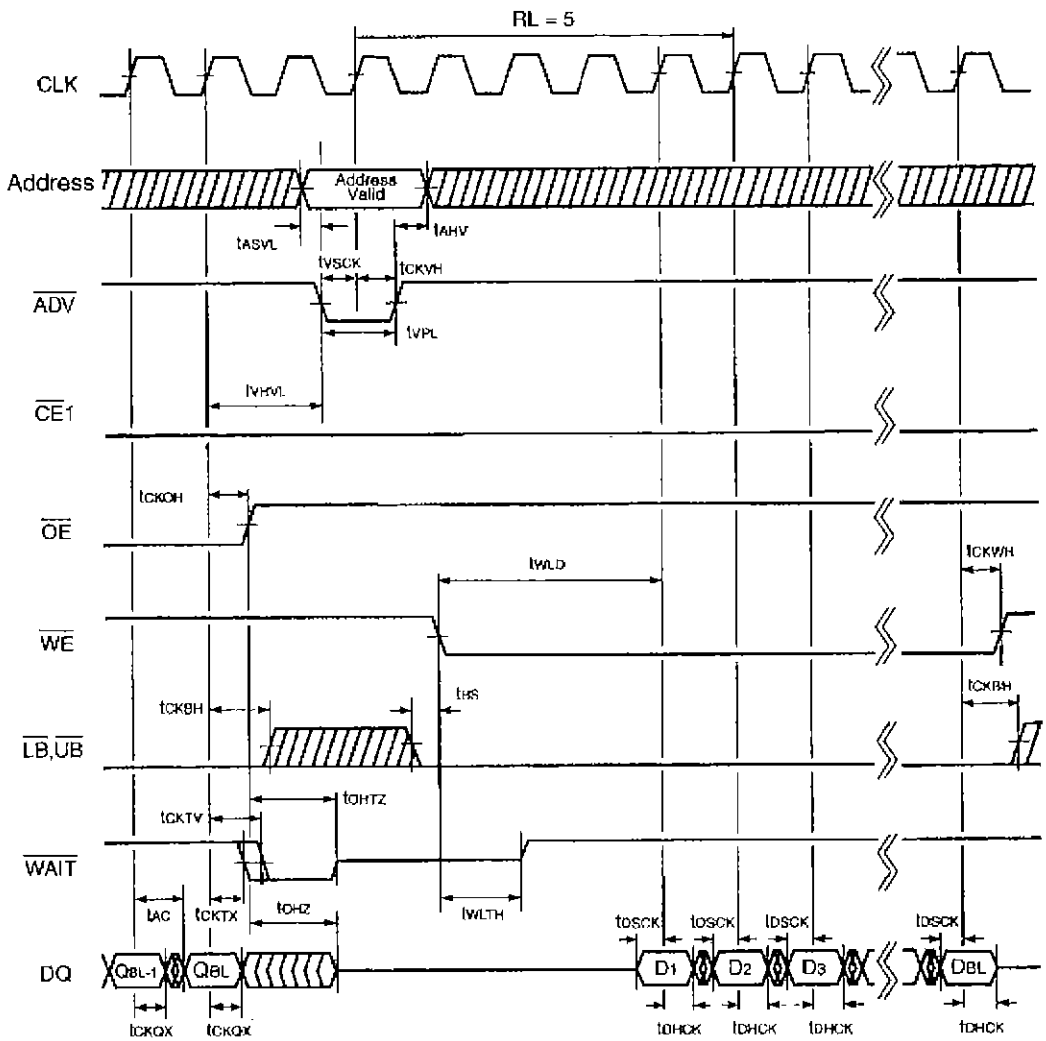
Notes : • This timing diagram assumes CE2 = H, the valid clock edge on rising edge and single write operation.
• Write data is latched on the valid clock edge.

(28) **Synchronous Read to Write Timing #1 ($\overline{CE}$1 Control)**



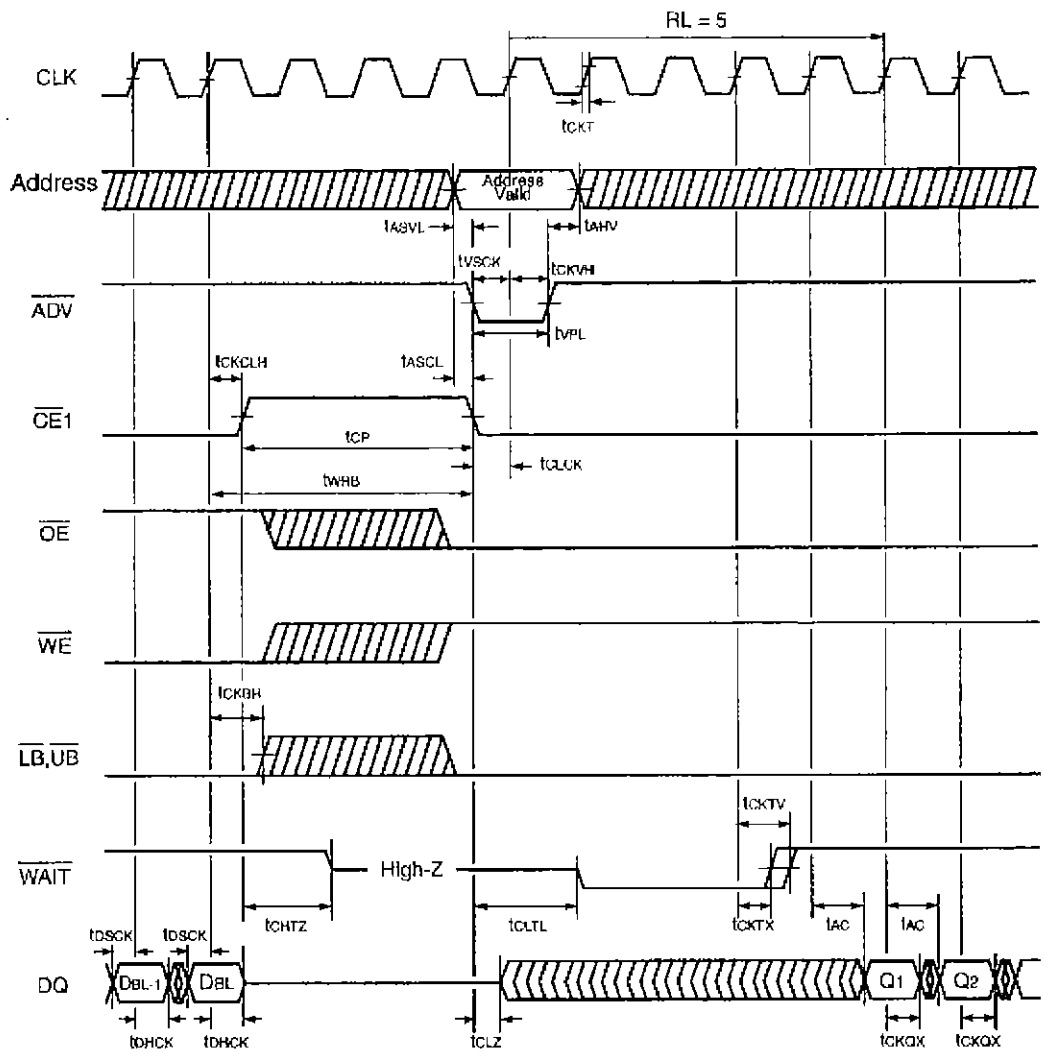
Note : This timing diagram assumes CE2 = H, the valid clock edge on rising edge and BL = 8 or 16.

(29) Synchronous Read to Write Timing #2 ($\overline{ADV}$ Control)



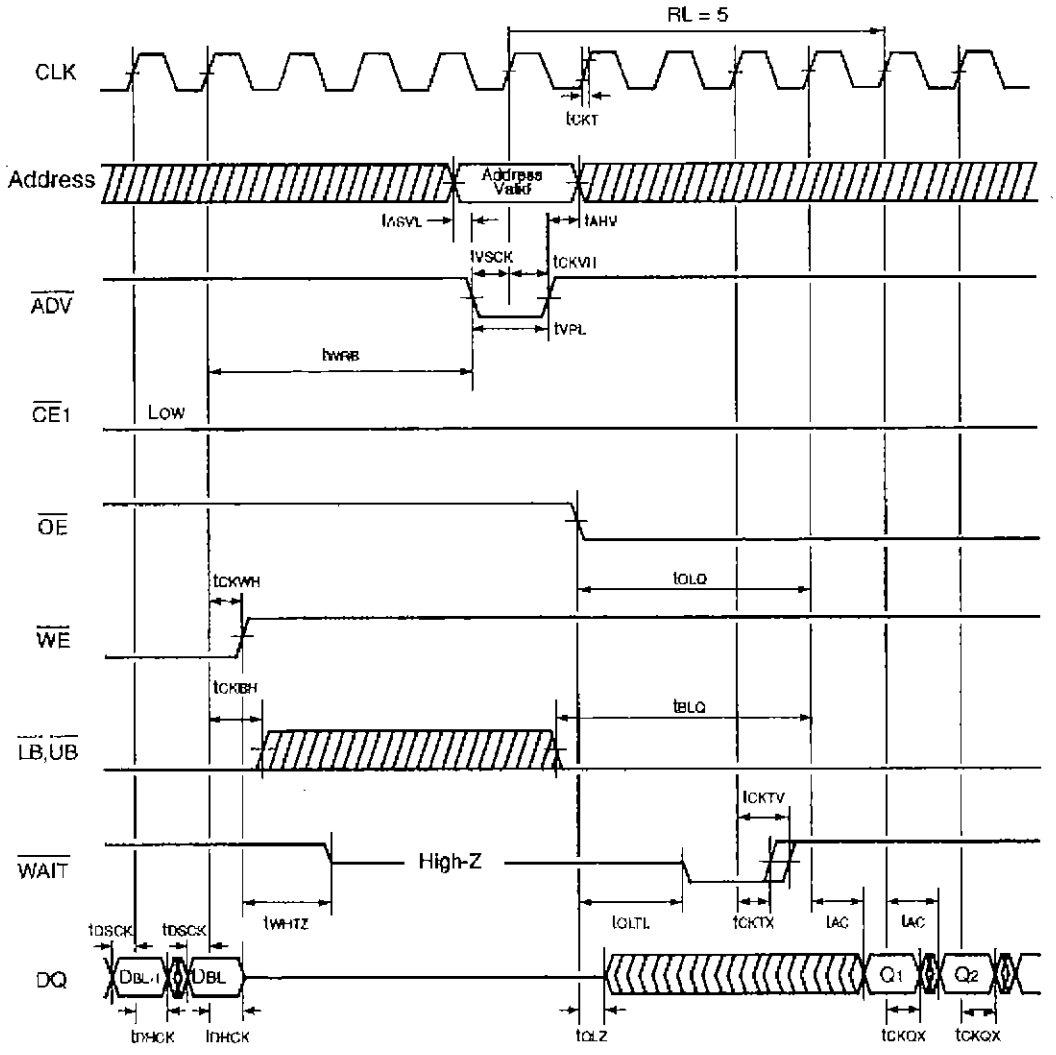
Note : This timing diagram assumes CE2 = H, the valid clock edge on rising edge and BL = 8 or 16.

(30) Synchronous Write to Read Timing #1($\overline{CE1}$ Control)



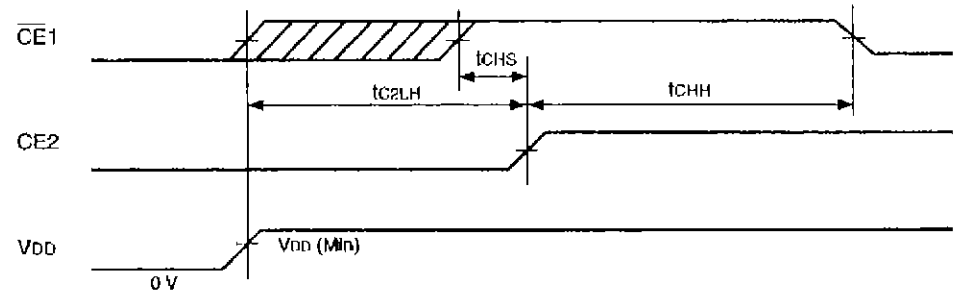
Note : This timing diagram assumes CE2 = H, the valid clock edge on rising edge and BL = 8 or 16.

(31) Synchronous Write to Read Timing #2 ($\overline{ADV}$ Control)



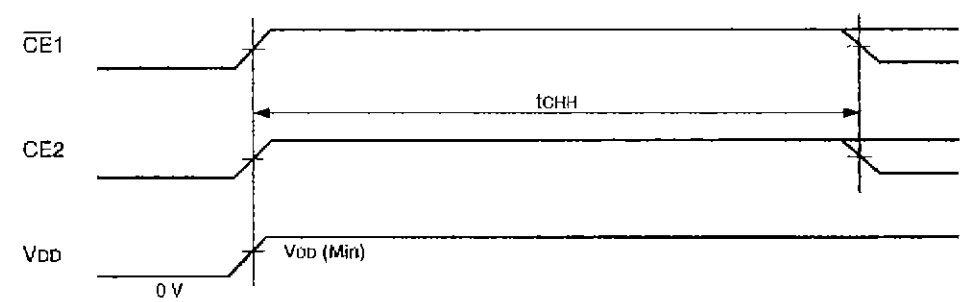
Note : This timing diagram assumes CE2 = H, the valid clock edge on rising edge and BL = 8 or 16.

(32) Power-up Timing #1



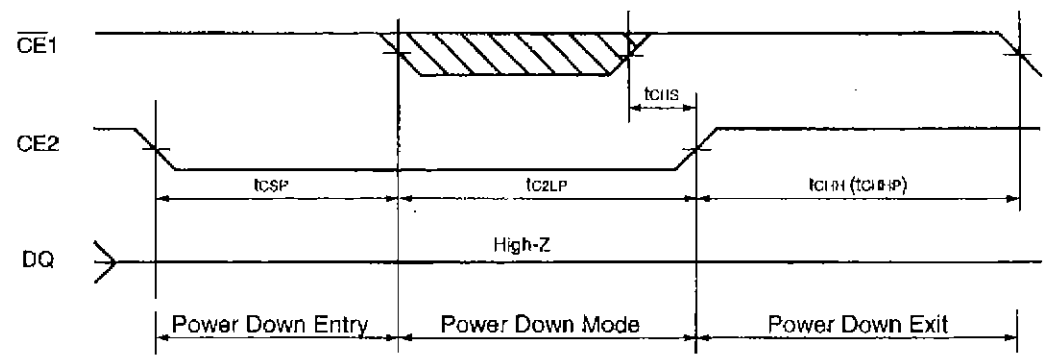
Note : The t_{C2LH} specifies after V_{DD} reaches specified minimum level.

(33) Power-up Timing #2



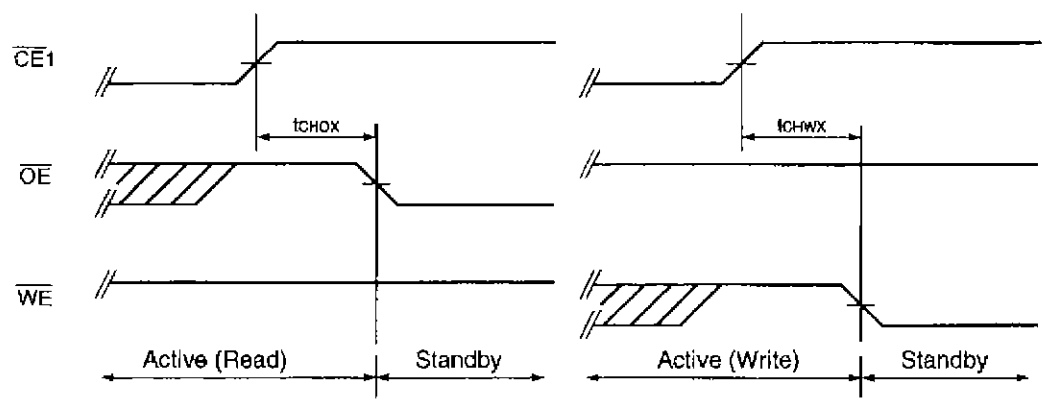
Note : The t_{CHH} specifies after V_{DD} reaches specified minimum level and applicable both $\overline{CE}1$ and CE2. If transition time of V_{DD} (from 0 V to V_{DD} (Min)) is longer than 50 ms, Power-up Timing #1 must be applied.

(34) Power Down Entry and Exit Timing



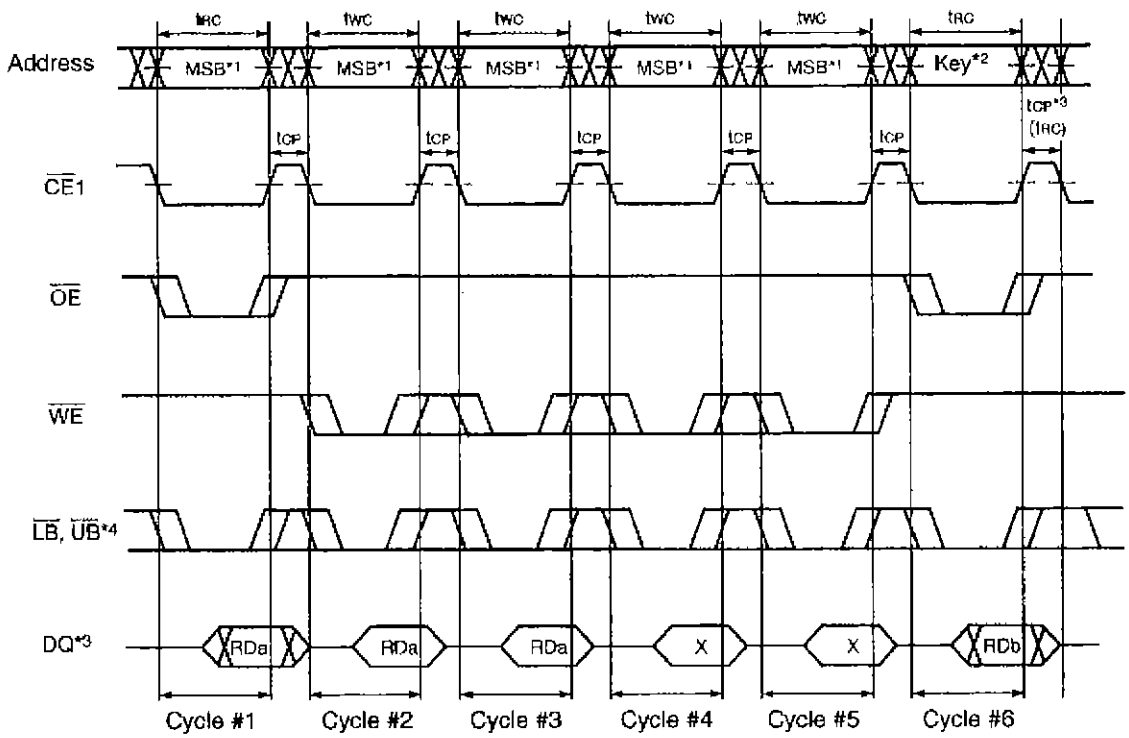
Note : This Power Down mode can be also used as a reset timing if "Power-up timing" above could not be satisfied and Power Down program was not performed prior to this reset.

(35) Standby Entry Timing after Read or Write



Note : Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode.

(36) Configuration Register Set Timing #1 (Asynchronous Operation)



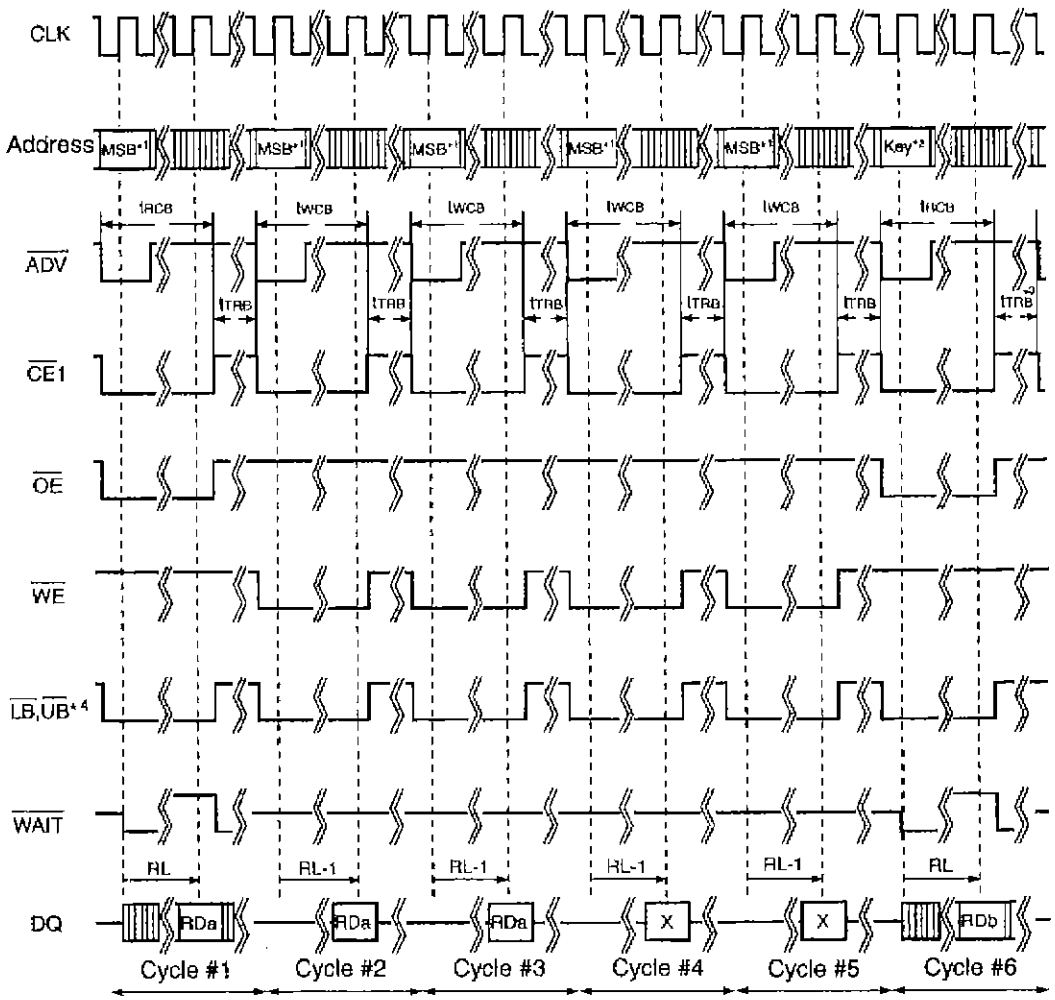
*1 : The all address inputs must be High from Cycle #1 to #5.

*2 : The address key must confirm the format specified in "■FUNCTIONAL DESCRIPTION". If not, the operation and data are not guaranteed.

*3 : After t_{CP} or t_{RC} following Cycle #6, the Configuration Register Set is completed and returned to the normal operation. t_{CP} and t_{RC} are applicable to returning to asynchronous mode and to synchronous mode respectively.

*4 : Byte read or write is available in addition to Word read or write. At least one byte control signal ($\overline{LB}$ or $\overline{UB}$) need to be Low.

(37) Configuration Register Set Timing #2 (Synchronous Operation)



*1 : The all address inputs must be High from Cycle #1 to #5.

*2 : The address key must confirm the format specified in "■FUNCTIONAL DESCRIPTION". If not, the operation and data are not guaranteed.

*3 : After t_{TRB} following Cycle #6, the Configuration Register Set is completed and returned to the normal operation.

*4 : Byte read or write is available in addition to Word read or write. At least one byte control signal ($\overline{LB}$ or $\overline{UB}$) need to be Low.

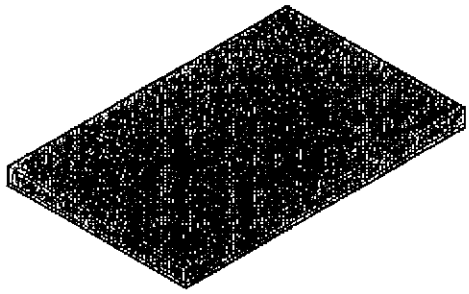
■ BONDING PAD INFORMATION

Please contact local FUJITSU representative for pad layout and pad coordinate information.

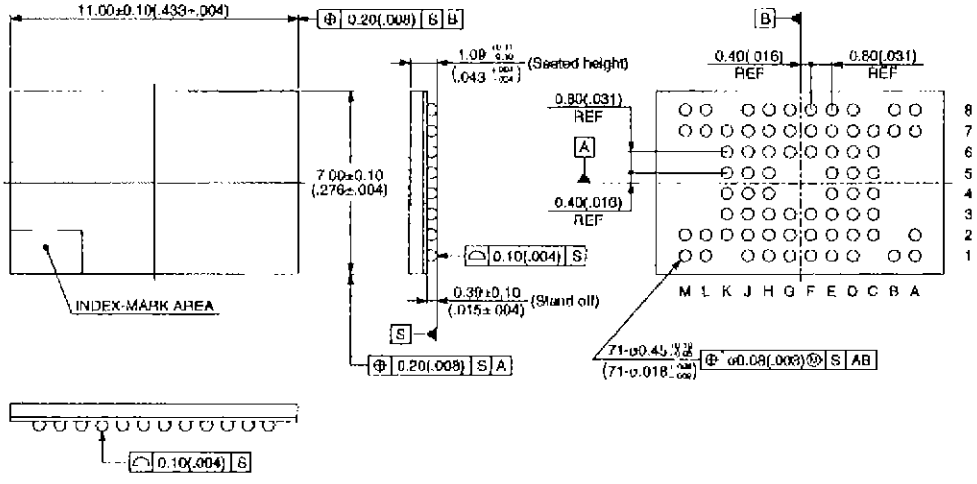
■ ORDERING INFORMATION

Part Number	Shipping Form / Package	Remarks
MB82DBS02163C-70LWT	wafer	
MB82DBS02163C-70LPBT	71-ball plastic FBGA (BGA-71P-M03)	

■ PACKAGE DIMENSION

71-ball plastic FBGA		
	Ball pitch	0.80 mm
	Package width × package length	7.00 × 11.00 mm
	Lead shape	Soldering ball
	Sealing method	Plastic mold
	Ball size	Ø0.45 mm
	Mounting height	1.20 mm Max.
(BGA-71P-M03)	Weight	0.14 g

71-ball plastic FBGA
(BGA-71P-M03)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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Edited Business Promotion Dept.

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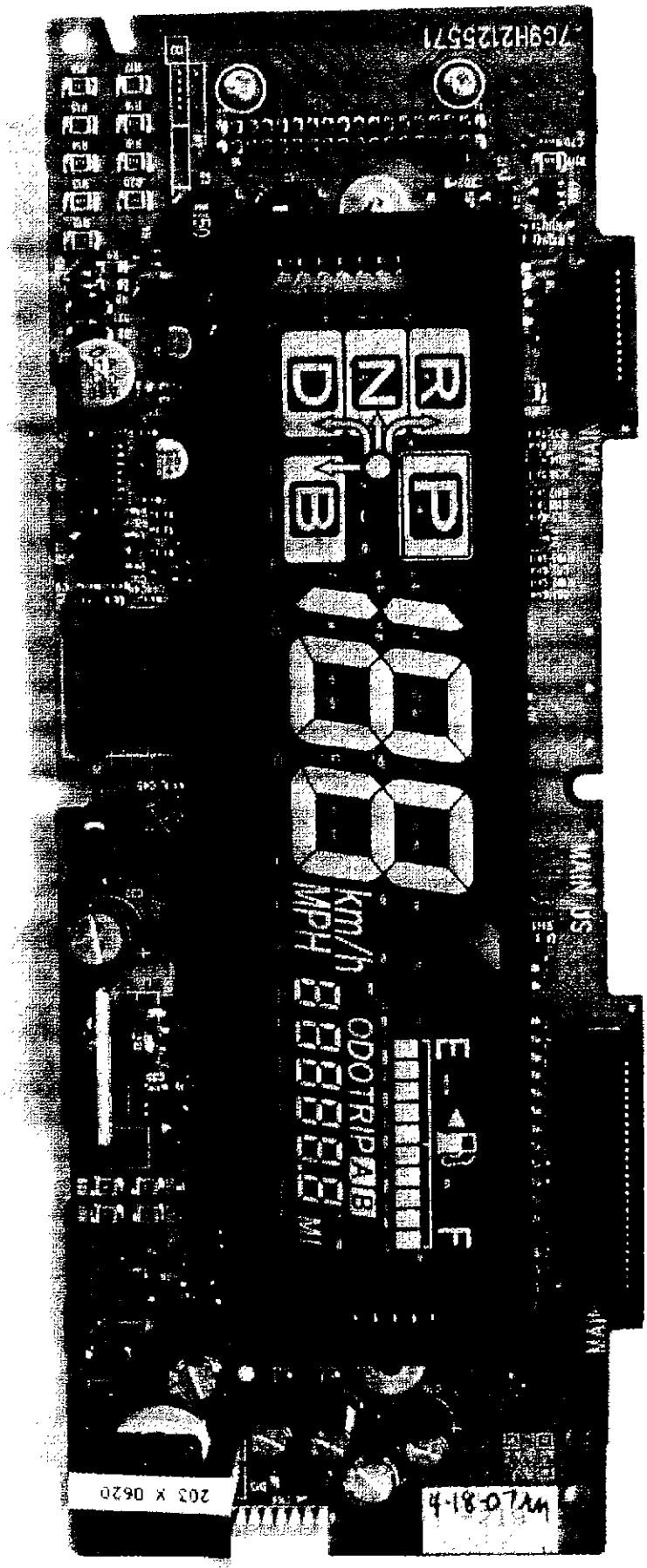
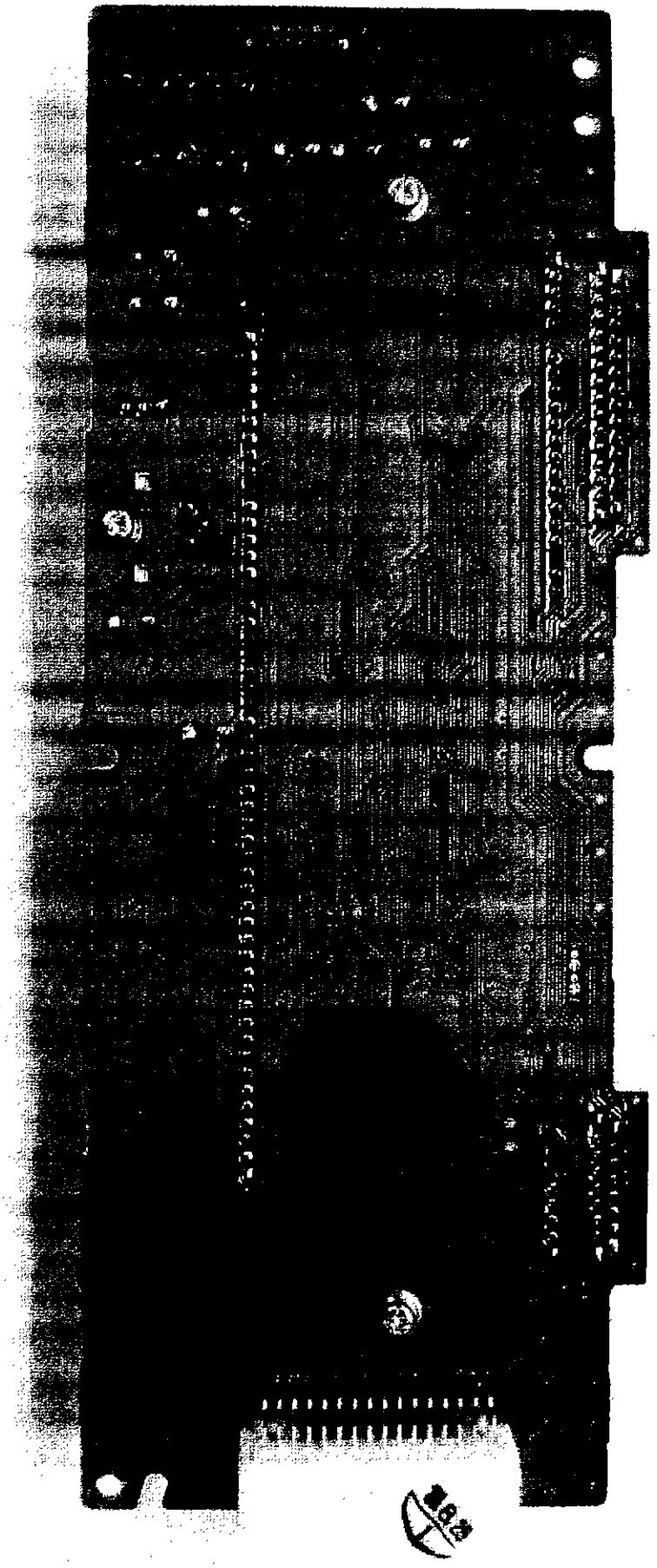
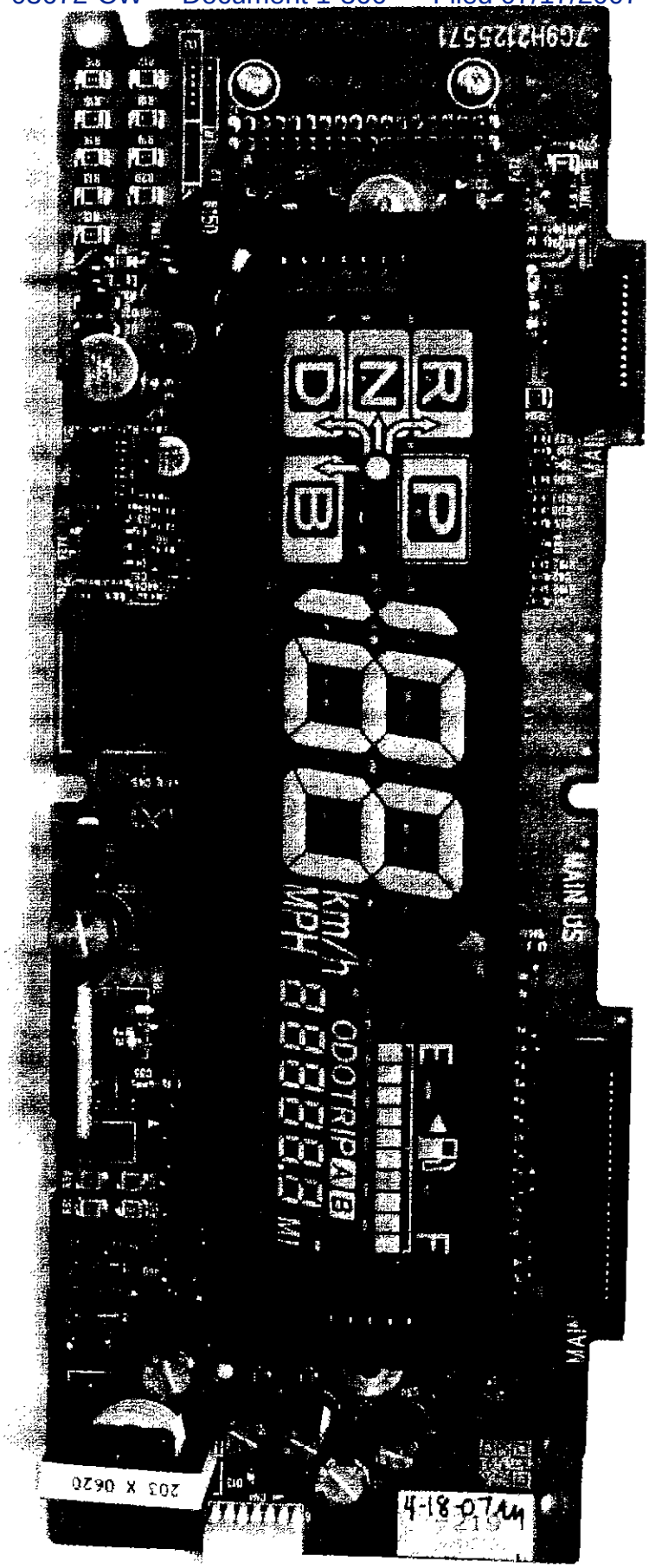
EXHIBIT F


km/h
MPH
ODO TRIP A B
E
F
203 X 0620




MAIN US
MAIN
km/h MPH
ODO TRIP A B
203 X 0620
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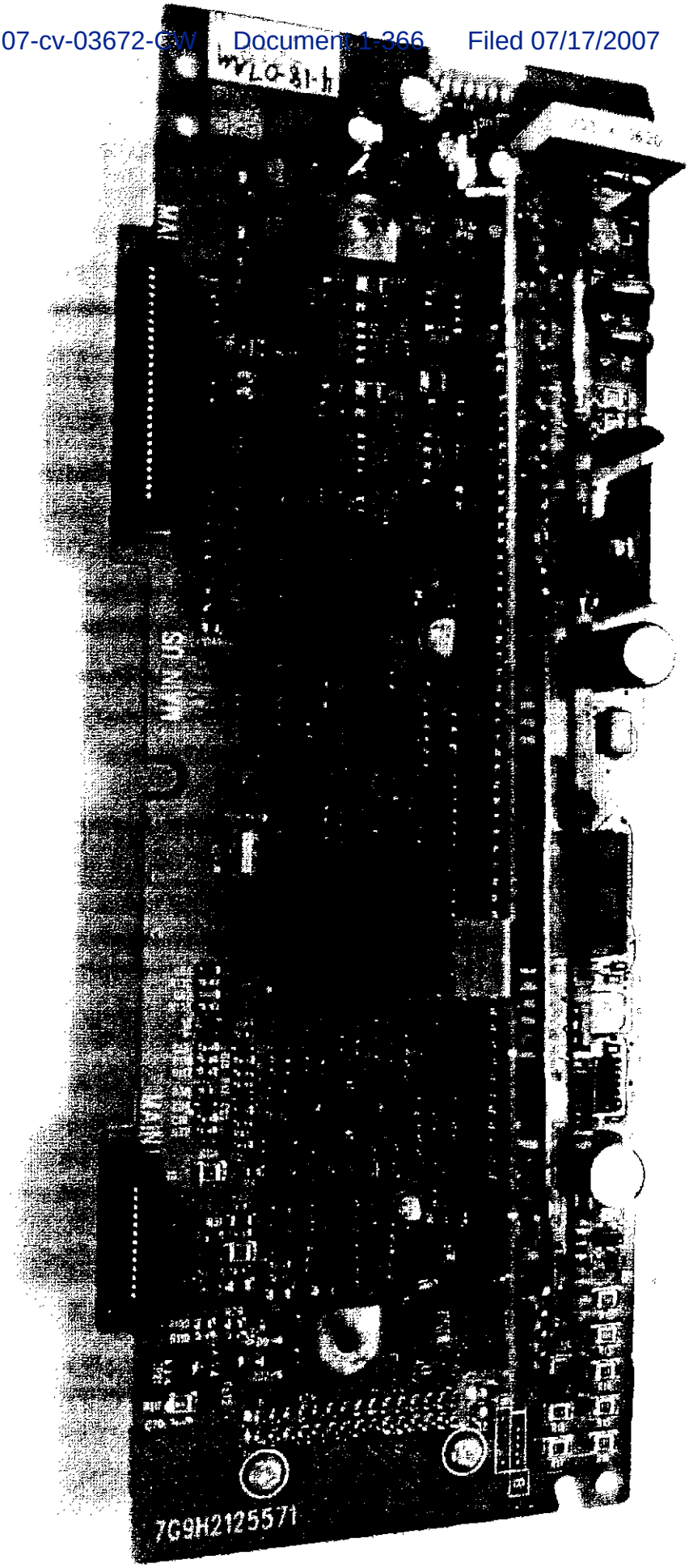
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